#12 Translation
2/12/03

Attorney Docket No : 215544US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Takuji MATSUMOTO, et al.)

Application Serial No.:)
09/986,004)

Filing Date:)
November 7, 2001)

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME)

VERIFICATION OF TRANSLATION

Honorable Commissioner of
Patents and Trademarks
Washington D.C. 20231

Sir:

Kanae JOMA residing at c/o Yoshida, Yoshitake and Arita Patent Office of Sumitomo-Seimei OBP Plaza Building, 4-70, Shiromi 1-chome, Chuo-ku, Osaka, Japan

declares:

1) that I know well both the Japanese and English languages;

2) that I translated the priority document of Japanese Patent Application No. P2001-035180 from Japanese to English;

3) that the attached English translation is a true and correct translation of the priority document of Japanese Patent Application No. P2001-035180 to the best of my knowledge and belief; and

4) that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: Jan. 28, 2003

Signature: Kanae Joma

Kanae JOMA

PATENT OFFICE

JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this office.

Date of Application: February 13, 2001

Patent Application Number: P2001-035180

Applicant(s): MITSUBISHI DENKI KABUSHIKI KAISHA

Commissioner,

Patent Office

[Document Name] Patent Application
[Docket Number] 528721JP01
[Filing Date] February 13, 2001
[Directed to] To the Director General of the J.P.O.
[International Patent Category] H01L 27/12
[Inventor]
[Domicile] c/o MITSUBISHI DENKI KABUSHIKI KAISHA, 2-3 Marunouchi 2-chome, Chiyoda-ku, TOKYO JAPAN
[Name] Takuji MATSUMOTO
[Inventor]
[Domicile] c/o MITSUBISHI DENKI KABUSHIKI KAISHA, 2-3 Marunouchi 2-chome, Chiyoda-ku, TOKYO JAPAN
[Name] Shigenobu MAEDA
[Inventor]
[Domicile] c/o MITSUBISHI DENKI KABUSHIKI KAISHA, 2-3 Marunouchi 2-chome, Chiyoda-ku, TOKYO JAPAN
[Name] Toshiaki IWAMATSU
[Inventor]
[Domicile] c/o MITSUBISHI DENKI KABUSHIKI KAISHA, 2-3 Marunouchi 2-chome, Chiyoda-ku, TOKYO JAPAN
[Name] Takashi IPPOSHI
[Applicant of Patent Application]
[Identification Number] 000006013
[Name] MITSUBISHI DENKI KABUSHIKI KAISHA
[Attorney]
[Identification Number] 100089233
[Patent Attorney]
[Name] Shigeaki YOSHIDA
[Attorney]
[Identification Number] 100088672
[Patent Attorney]
[Name] Hidetoshi YOSHITAKE
[Attorney]
[Identification Number] 100088845

[Patent Attorney]
[Name] Takahiro ARITA
[Government Fee]
[Prepayment Ledger Number] 012852
[Fee] 21,000 yen
[List of Attached Items]

[Item]	Specification	1
[Item]	Drawings	1
[Item]	Abstract of the Disclosure	1

[Necessity of Proof] Yes

[Document Name] SPECIFICATION

[Title of the Invention] Semiconductor Device and Method of Manufacturing the Same

[Scope of Claim for Patent]

[Claim 1] A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprising:

a MOS transistor provided in an element formation region of said SOI layer; and

a partial isolation region provided in said SOI layer for isolating said element formation region, said partial isolation region including a partial insulation film provided in an upper portion of said SOI layer, and an under-partial-insulation-film semiconductor region provided in a lower portion of said SOI layer, said under-partial-insulation-film semiconductor region being a part of said SOI layer,

said MOS transistor including:

source and drain regions of a first conductivity type each selectively formed in said SOI layer;

a gate electrode having a gate electrode main part formed on a region of said SOI layer between said source and drain regions, with a gate oxide film provided between said gate electrode main part and said region of said SOI layer; and

a body region having a body region main part which is a region of a second conductivity type of said SOI layer between said source and drain regions, and a body region potential setting portion formed in said element formation region and electrically connected from said body region main part, the electrical potential of said body region potential setting portion being externally fixable.

[Claim 2] The semiconductor device according to claim 1, wherein

said body region potential setting portion includes a body region source/drain

adjacent portion adjacent to said source and drain regions in a gate width direction and extending in a gate length direction from said body region main part; and

said gate electrode further has a gate extension region extending in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, said gate extension region electrically shutting off said body region source/drain adjacent portion and said source and drain regions.

[Claim 3] The semiconductor device according to claim 2, wherein

said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extending in a first direction from said body region main part and a second body region source/drain adjacent portion extending in a second direction opposite from said first direction from said body region main part, and

said gate extension region includes a first gate extension region formed on said first body region source/drain adjacent portion and a first gate extension region formed on said second body region source/drain adjacent portion.

[Claim 4] The semiconductor device according to claim 2, wherein

said body region source/drain adjacent portion includes one body region source/drain adjacent portion, and

said gate extension region includes one gate extension region formed on said one body region source/drain adjacent portion.

[Claim 5] The semiconductor device according to any one of claims 2 through 4, wherein

said body region source/drain adjacent portion has a high concentration region of the second conductivity type having an impurity concentration higher than that of other regions, said high concentration region being spaced a predetermined distance apart from said gate extension region.

[Claim 6] The semiconductor device according to any one of claims 2 through 4, wherein

said gate extension region includes a gate extension region of the second conductivity type having an impurity concentration of not greater than 5×10^{18} cm^{-2}.

[Claim 7] The semiconductor device according to any one of claims 1 through 5, wherein

said body region potential setting portion includes a body-fixing semiconductor region of the second conductivity type formed together with said source region.

[Claim 8] The semiconductor device according to any one of claims 1 through 7, wherein

said under-partial-isolation-film semiconductor region is of the second conductivity type and is formed in contact with said body region,

said semiconductor device further comprising

an outside-element-formation-region body region of the first conductivity type provided outside said element formation region of said SOI layer, the electric potential of said outside-element-formation-region body region being externally fixable, said outside-element-formation-region body region being formed in contact with said under-partial-insulation-film semiconductor region.

[Claim 9] The semiconductor device according to any one of claims 1 through 8, wherein

said source and drain regions have such depths as to reach said buried insulation layer.

[Claim 10] The semiconductor device according to any one of claims 1 through 8, wherein

said source and drain regions have such depths that a depletion layer extending

from said source and drain regions does not reach said buried insulation layer during a normal operation.

[Claim 11] The semiconductor device according to any one of claims 1 through 8, wherein

said source and drain regions do not reach said buried insulation layer, and a depletion layer extending from said drain region has such a depth as to reach said buried insulation layer during a normal operation.

[Claim 12] The semiconductor device according to any one of claims 1 through 8, wherein

said drain region has a depth greater than that of said source region, and the depth of said drain region is such that a depletion layer extending from said drain region reaches said buried insulation layer during a normal operation.

[Claim 13] A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprising:

first and second semiconductor regions of a predetermined conductivity type provided in an element formation region of said SOI layer; and

a partial insulation film provided in an upper portion of said element formation region, and an under-partial-insulation-film semiconductor region of a predetermined conductivity type provided in a lower portion of said element formation region, said under-partial-insulation-film semiconductor region being a part of said element formation region,

wherein said under-partial-insulation-film semiconductor region is electrically connected to said first and second semiconductor regions to constitute a resistive element.

[Claim 14] The semiconductor device according to claim 13, further comprising

a complete insulation film provided through said SOI layer for isolating said element formation region.

[Claim 15] The semiconductor device according to claim 13 or 14, wherein

said element formation region except in said partial insulation film and said first and second semiconductor regions is a part of a region where said resistive element is to be formed.

[Claim 16] The semiconductor device according to any one of claims 13 through 15, wherein

said resistive element includes a load resistor of an SRAM memory cell.

[Claim 17] A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprising:

first and second element formation regions provided in said SOI layer;

a partial isolation region including a partial insulation film provided in an upper portion of said SOI layer and a semiconductor region provided under said partial insulation film, said semiconductor region being a part of said SOI layer, said partial isolation region for providing isolation between said first and second element formation regions; and

first and second MOS transistors formed in said first and second element formation regions, respectively,

wherein said first and second MOS transistors are made different from each other in at least one of a body region structure, a gate electrode structure and the presence/absence of body potential fixation, thereby to have different transistor characteristics.

[Claim 18] A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprising:

first and second element formation regions provided in said SOI layer;

a partial isolation region including a partial insulation film provided in an upper portion of said SOI layer and a semiconductor region provided under said partial insulation film, said semiconductor region being a part of said SOI layer, said partial isolation region for isolating said first element formation region from other regions;

a complete isolation region including a complete insulation film provided through said SOI layer for isolating said second element formation region from other regions;

a first MOS transistor formed in said first element formation region; and

a second MOS transistor formed in said second element formation region,

wherein said first and second MOS transistors have different transistor characteristics.

[Claim 19] A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing an SOI substrate having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer;

(b) selectively forming a partial insulation film in an upper portion of said SOI layer, said partial insulation film, in conjunction with a semiconductor region, constituting a partial isolation region for providing isolation between first and second element formation regions in said SOI layer, said semiconductor region being provided under said partial insulation film and being a part of said SOI layer; and

(c) forming first and second MOS transistors in said first and second element formation regions, respectively,

wherein, in said step (c), said first and second MOS transistors are made different from each other in at least one of a body region structure, a gate electrode

structure and the presence/absence of body potential fixation, thereby to have different transistor characteristics.

[Claim 20] A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing an SOI substrate having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer;

(b) selectively forming a partial insulation film in an upper portion of said SOI layer, said partial insulation film, in conjunction with a semiconductor region, constituting a partial isolation region for isolating said first element formation region from other regions, said semiconductor region being provided under said partial insulation film and being a part of said SOI layer;

(c) selectively forming a complete insulation film through said SOI layer, said complete insulation film constituting a complete isolation region for isolating said second element formation region from other regions;

(d) forming a first MOS transistor in said first element formation region; and

(e) forming a second MOS transistor in said second element formation region,

wherein, in said steps (d) and (e), said first and second MOS transistors are formed to have different transistor characteristics.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device having an SOI structure and a method of manufacturing the semiconductor device.

[0002]

[Prior Art]

Attention has recently been paid to a semiconductor device referred to as an SOI (Silicon-On-Insulator) device since it is a high-speed low-power-consumption device.

[0003]

The SOI device is fabricated on an SOI substrate having an SOI structure in which a buried oxide film is provided between an SOI layer and a silicon substrate. In particular, an SOI device in which the SOI layer serving as an upper silicon layer is reduced in thickness (to approximately several micrometers (μm)) is referred to as a thin film SOI device which has received attention and been expected for application to LSI circuits for portable equipment. Conventionally, an SOI element (a (semiconductor) element formed in the SOI layer having the SOI structure) is completely isolated by an isolation oxide film extending through Si (silicon) of the SOI layer to the buried oxide film.

[0004]

[Problems to be Solved by the Invention]

The complete isolation technique is advantageous in being latchup free (or causing no latchup) and having high resistance to noises because the element is electrically completely insulated from other elements. However, since a transistor operates in an electrically floating state, there are problems in frequency dependence of delay time and in a floating-body effect, for example, a kink effect which exhibits a hump on a drain current-drain voltage characteristic or the like. To suppress the floating-body effect, a partial isolation technique is effective which includes: forming an isolation oxide film (partial oxide film) in an upper portion out of contact with the buried oxide film; constituting a partial isolation region together with a part of an SOI layer in a lower portion; and providing a body terminal in a body region formed in a region isolated by the

partial isolation region, thereby to fix the substrate potential (body potential) through the SOI layer provided under the partial oxide film. However, there is a problem in that the partial isolation technique does not have the advantage of being latchup free which is the advantage of the complete isolation technique.

[0005]

Therefore, there has been developed a partial isolation and complete isolation combination technique having both advantages. In the partial isolation and complete isolation combination technique, different trench depths are used for the partial isolation and complete isolation combination. For this reason, after an oxide film of an isolation oxide film is deposited and is then subjected to a CMP process, dishing occurs in a complete isolation portion having a greater trench depth in contrast with the partial isolation. Accordingly, there is a difference in the shape of an important isolation edge for the reliability of a gate oxide film between the partial isolation and the complete isolation. In the combination process, the isolation edge of the complete isolation is lower, so that a threshold voltage of a MOS transistor is locally dropped in an edge portion. Therefore, there is apprehension that a leakage current increases.

[0006]

In only the conventional device, transistors have different distances from the body terminals. This causes variations in body resistance, resulting in variations in threshold voltage.

[0007]

In addition, there is a problem in that the partial isolation technique for fixing the body potential through the SOI layer provided under the partial oxide film cannot fix the body potential with high stability.

[0008]

The present invention has been made to solve the above-mentioned problems. It is therefore an object of the present invention to provide a semiconductor device having an SOI structure which can fix a body potential with high stability in a body region in an element formation region isolated by a partial isolation region, and to provide a semiconductor device capable of constituting a high functional semiconductor integrated circuit when partial isolation or a partial isolation and complete isolation combination is carried out, and a method of manufacturing the same.

[0009]

[Means for Solving the Problems]

[Claim 1] According to claim 1 of the present invention, a semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer comprises: a MOS transistor provided in an element formation region of said SOI layer; and a partial isolation region provided in said SOI layer for isolating said element formation region, said partial isolation region including a partial insulation film provided in an upper portion of said SOI layer, and an under-partial-insulation-film semiconductor region provided in a lower portion of said SOI layer, said under-partial-insulation-film semiconductor region being a part of said SOI layer, said MOS transistor including: source and drain regions of a first conductivity type each selectively formed in said SOI layer; a gate electrode having a gate electrode main part formed on a region of said SOI layer between said source and drain regions, with a gate oxide film provided between said gate electrode main part and said region of said SOI layer; and a body region having a body region main part which is a region of a second conductivity type of said SOI layer between said source and drain regions, and a body region potential setting portion formed in said element formation region and electrically connected from said body region main part, the electrical potential of said

body region potential setting portion being externally fixable.

[0010]

According to claim 2 of the invention, in the semiconductor device defined in claim 1, said body region potential setting portion includes a body region source/drain adjacent portion adjacent to said source and drain regions in a gate width direction and extending in a gate length direction from said body region main part; and said gate electrode further has a gate extension region extending in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, said gate extension region electrically shutting off said body region source/drain adjacent portion and said source and drain regions.

[0011]

According to claim 3 of the invention, in the semiconductor device defined in claim 2, said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extending in a first direction from said body region main part and a second body region source/drain adjacent portion extending in a second direction opposite from said first direction from said body region main part, and said gate extension region includes a first gate extension region formed on said first body region source/drain adjacent portion and a first gate extension region formed on said second body region source/drain adjacent portion.

[0012]

According to claim 4 of the invention, in the semiconductor device defined in claim 2, said body region source/drain adjacent portion includes one body region source/drain adjacent portion, and said gate extension region includes one gate extension region formed on said one body region source/drain adjacent portion.

[0013]

According to claim 5 of the invention, in the semiconductor device defined in any one of claims 2 through 4, said body region source/drain adjacent portion has a high concentration region of the second conductivity type having an impurity concentration higher than that of other regions, said high concentration region being spaced a predetermined distance apart from said gate extension region.

[0014]

According to claim 6 of the invention, in the semiconductor device defined in any one of claims 2 through 4, said gate extension region includes a gate extension region of the second conductivity type having an impurity concentration of not greater than 5 x 10^{18} cm^{-2}.

[0015]

According to claim 7 of the invention, in the semiconductor device defined in any one of claims 1 through 5, said body region potential setting portion includes a body-fixing semiconductor region of the second conductivity type formed together with said source region.

[0016]

According to claim 8 of the invention, in the semiconductor device defined in any one of claims 1 through 7, said under-partial-isolation-film semiconductor region is of the second conductivity type and is formed in contact with said body region. The semiconductor device further comprises an outside-element-formation-region body region of the first conductivity type provided outside said element formation region of said SOI layer, the electric potential of said outside-element-formation-region body region being externally fixable, said outside-element-formation-region body region being formed in contact with said under-partial-insulation-film semiconductor region.

[0017]

According to claim 9 of the invention, in the semiconductor device defined in any one of claims 1 through 8, said source and drain regions have such depths as to reach said buried insulation layer.

[0018]

According to claim 10 of the invention, in the semiconductor device defined in any one of claims 1 through 8, said source and drain regions have such depths that a depletion layer extending from said source and drain regions does not reach said buried insulation layer during a normal operation.

[0019]

According to claim 11 of the invention, in the semiconductor device defined in any one of claims 1 through 8, said source and drain regions do not reach said buried insulation layer, and a depletion layer extending from said drain region has such a depth as to reach said buried insulation layer during a normal operation.

[0020]

According to claim 12 of the invention, in the semiconductor device defined in any one of claims 1 through 8, said drain region has a depth greater than that of said source region, and the depth of said drain region is such that a depletion layer extending from said drain region reaches said buried insulation layer during a normal operation.

[0021]

According to claim 13 of the invention, a semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprises: first and second semiconductor regions of a predetermined conductivity type provided in an element formation region of said SOI layer; and a partial insulation film provided in an upper portion of said element formation region, and an under-partial-insulation-film semiconductor region of a predetermined conductivity type

provided in a lower portion of said element formation region, said under-partial-insulation-film semiconductor region being a part of said element formation region, wherein said under-partial-insulation-film semiconductor region is electrically connected to said first and second semiconductor regions to constitute a resistive element.

[0022]

According to claim 14 of the invention, the semiconductor device defined in claim 13 further comprises a complete insulation film provided through said SOI layer for isolating said element formation region.

[0023]

According to claim 15 of the invention, in the semiconductor device defined in claim 13 or 14, said element formation region except in said partial insulation film and said first and second semiconductor regions is a part of a region where said resistive element is to be formed.

[0024]

According to claim 16 of the invention, in the semiconductor device defined in any one of claims 13 through 15, said resistive element includes a load resistor of an SRAM memory cell.

[0025]

According to claim 17 of the invention, a semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprises: first and second element formation regions provided in said SOI layer; a partial isolation region including a partial insulation film provided in an upper portion of said SOI layer and a semiconductor region provided under said partial insulation film, said semiconductor region being a part of said SOI layer, said partial isolation region for providing isolation between said first and second element formation regions; and first and

second MOS transistors formed in said first and second element formation regions, respectively, wherein said first and second MOS transistors are made different from each other in at least one of a body region structure, a gate electrode structure and the presence/absence of body potential fixation, thereby to have different transistor characteristics.

[0026]

According to claim 18 of the invention, a semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, comprises: first and second element formation regions provided in said SOI layer; a partial isolation region including a partial insulation film provided in an upper portion of said SOI layer and a semiconductor region provided under said partial insulation film, said semiconductor region being a part of said SOI layer, said partial isolation region for isolating said first element formation region from other regions; a complete isolation region including a complete insulation film provided through said SOI layer for isolating said second element formation region from other regions; a first MOS transistor formed in said first element formation region; and a second MOS transistor formed in said second element formation region, wherein said first and second MOS transistors have different transistor characteristics.

[0027]

According to claim 19 of the invention, a method of manufacturing a semiconductor device comprises the steps of: (a) preparing an SOI substrate having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer; (b) selectively forming a partial insulation film in an upper portion of said SOI layer, said partial insulation film, in conjunction with a semiconductor region, constituting a partial isolation region for providing isolation between first and second

element formation regions in said SOI layer, said semiconductor region being provided under said partial insulation film and being a part of said SOI layer; and (c) forming first and second MOS transistors in said first and second element formation regions, respectively, wherein, in said step (c), said first and second MOS transistors are made different from each other in at least one of a body region structure, a gate electrode structure and the presence/absence of body potential fixation, thereby to have different transistor characteristics.

[0028]

According to claim 20 of the invention, a method of manufacturing a semiconductor device comprises the steps of: (a) preparing an SOI substrate having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer; (b) selectively forming a partial insulation film in an upper portion of said SOI layer, said partial insulation film, in conjunction with a semiconductor region, constituting a partial isolation region for isolating said first element formation region from other regions, said semiconductor region being provided under said partial insulation film and being a part of said SOI layer; (c) selectively forming a complete insulation film through said SOI layer, said complete insulation film constituting a complete isolation region for isolating said second element formation region from other regions; (d) forming a first MOS transistor in said first element formation region; and (e) forming a second MOS transistor in said second element formation region, wherein, in said steps (d) and (e), said first and second MOS transistors are formed to have different transistor characteristics.

[0029]

[Embodiments of the Invention]

<Overview of the Invention>

(Technical Background)

A partial isolation technique has an advantage in being capable of externally setting the electric potential of a body region provided outside an element formation region by means of a partial isolation region, thereby to fix a substrate potential through an SOI layer provided under a partial oxide film. The advantage is not always sufficient for a high breakdown voltage element or a device requiring high reliability of hot carriers. Since the SOI layer provided under the partial oxide film has a small thickness, a finite body resistance is present. Also in the device, therefore, a kink sometimes occurs because of the body resistance in a high voltage region. Consequently, the partial isolation technique has a technical background in that the reliability of hot carriers and the frequency dependence of delay time are not always sufficient.

[0030]

To prevent the degradation of the reliability of a gate oxide film due to different isolation edges in the partial isolation technique or a partial isolation and complete isolation combination technique, there is a need for a semiconductor device which uses an H gate electrode and a T gate electrode to be described below in detail in a portion where the reliability is particularly required, thereby to improve the reliability for body potential fixation and to suppress the increase in edge leakage current.

[0031]

(Single Type of Transistor)

In partial isolation having a body terminal, the use of a single type of transistor using one of an H gate electrode, a T gate electrode and a source-tied structure which will be described below in detail further improves the stability for fixing the body potential to further improve the problems of hot carriers and the frequency dependence of delay time. By such a method, however, the speed of a circuit is reduced. Therefore, it is desirable

that a conventional device (a device using a gate electrode having an ordinary structure or the like) should be utilized in a portion where a high speed is required.

[0032]

(Combination of Plural Types of Transistors)

Moreover, when a body terminal is not partially provided and a transistor is operated in a floating state, a threshold voltage can be dropped. Therefore, a transistor having a large drain current can be fabricated. Accordingly, the provision of a transistor having a body floating structure in a circuit together with a transistor having a body fixing structure by means of the body terminal allows the fabrication of a high-speed low-power-consumption circuit.

[0033]

In the partial isolation technique, threshold variations due to a difference in distance from the body terminal can be suppressed by the use of the H gate electrode, the T gate electrode and the source-tied structure in which the body terminal is to be provided in respective transistors. Furthermore, when a floating structure using no body terminal is utilized, it is apparent that the threshold variations due to a body resistance can be suppressed. The floating structure has a disadvantage in that a threshold voltage has frequency dependence.

[0034]

Combination of plural types of transistors having various features provides a high functional device in respect of design.

[0035]

<First Embodiment>

(Conventional PDSOI-MOSFET)

Fig. 1 is a sectional view showing an example of a PD (Paially-Depleted)

SOI-MOSFET which is one of the conventional MOS transistors, and Fig. 2 is a plan view showing an example of the conventional PDSOI-MOSFET. A section taken along the line A1-A1 in Fig. 2 corresponds to Fig. 1.

[0036]

The PDSOI-MOSFET has such a feature that a depletion layer 90 directly under a gate electrode 7 does not reach a buried oxide film 2 as shown in Fig. 1. Because of such a feature, the PDSOI-MOSFET has an excellent controllability of the threshold voltage.

[0037]

As shown in Figs. 1 and 2, an SOI layer 4 is formed on the buried oxide film 2 formed on a semiconductor substrate (not shown), whereby an SOI substrate having an SOI structure is implemented. The SOI layer 4 is isolated by a partial isolation region including a partial oxide film 31 and a p well region 11 provided under the partial oxide film 31.

[0038]

A source region 51 and a drain region 61 which are selectively formed in the SOI layer 4 have such depths as to reach a back face of the SOI layer 4 (a surface of the buried oxide film 2) from a surface thereof.

[0039]

A gate oxide film 5 is formed on the SOI layer 4 between the source region 51 and the drain region 61, and the gate electrode 7 is formed on the gate oxide film 5. Side walls 6 are formed on side surfaces of the gate electrode 7. Then, a source terminal 26 and a drain terminal 27 are provided on the source region 51 and the drain region 61, respectively.

[0040]

A body region 10 (an outside-element-formation-region body region) is isolated by the partial oxide film 31 an the p well region 11 provided thereunder and is formed to extend from the surface of the SOI layer 4 to the back face thereof. The body region 10 is electrically connected to a body region main part which is part of the SOI layer 4 provided under the gate electrode 7 through the p well region 11.

[0041]

Application of a predetermined electric potential to a body terminal 25 provided on the body region 10 for body fixing of the PDSOI-MOSFET shown in Fig. 1 (fixing of a channel potential in the SOI layer 4 provided under the gate oxide film 5) suppresses the above-mentioned floating effect.

[0042]

(PDSOI-MOSFET according to First Embodiment)

Fig. 3 is a plan view showing a planar structure of a semiconductor device according to a first embodiment of the present invention, Fig. 4 is a sectional view showing a section taken along the line A2-A2 of Fig. 3, and Fig. 5 is a sectional view showing a section taken along the line B1-B1 of Fig. 3.

[0043]

The semiconductor device according to the first embodiment is provided on an SOI layer isolated partially and provides body fixation through a PDSOI-MOSFET having an H gate electrode.

[0044]

As shown in Fig. 3, an H gate electrode 71 has left and right (in the figure, upper and lower) "I"s (a gate extension region or first and second body region source/drain adjacent portions) for electrically isolating body regions 13 formed adjacent in a gate width W direction to the source region 51 and the drain region 61 from the drain

region 61 and the source region 51, and a central "–" (a gate electrode main part) functioning as a gate electrode of an original MOS transistor. A p^- body region is formed under the each of the left and right (in the figure, upper and lower) "I"s of the H gate electrode 71, with an insulation film therebetween.

[0045]

As shown in Figs. 3 and 5, two body regions 13, 13 (the first and second body region source/drain adjacent portions) extend in a first direction along the gate length and a second direction opposite therefrom from the body region main part which is part of the SOI layer 4 under the gate electrode main part of the H gate electrode 71, and are adjacent in the gate width direction to the source region 51 and the drain region 61.

[0046]

Thus, the left and right "I"s of the H gate electrode 71 electrically cut off the source region 51 and drain region 61 from the body regions 13, 13 to prevent the body potential obtained from body terminals 28 from being directly transmitted to the drain region 61 and the source region 51.

[0047]

The source region 51 and the drain region 61 which are selectively formed in the SOI layer 4 have such depths as to reach the back face of the SOI layer 4 from the surface thereof.

[0048]

The gate oxide film 5 is formed on the SOI layer 4 between the source region 51 and the drain region 61, and the central "–" portion of the H gate electrode 71 is formed on the gate oxide film 5. The side walls 6 are formed on the side surfaces of the H gate electrode 71. Then, the source terminal 26 and the drain terminal 27 (not shown in Fig. 4) are provided on the source region 51 and the drain region 61, respectively.

[0049]

The body regions 10 are isolated by the partial isolation region including the partial oxide film 31 and the p well region 11 provided thereunder and are formed to extend from the surface of the SOI layer 4 to the back face thereof. The body regions 10 are electrically connected to the body region main part which is part of the SOI layer 4 provided under the gate electrode 71 through the p well region 11.

[0050]

As described above, the body regions 13 are adjacent to the body region main part (the channel region) which is part of the SOI layer 4 provided under the gate oxide film 5.

[0051]

Application of a predetermined electric potential to the body terminals 28 provided on the body region 13 in addition to the body terminals 25 provided on the body regions 10 accomplishes the body fixation of the PDSOI-MOSFET according to the first embodiment. Therefore, the body potential or the electric potential of the body region main part can be fixed stably so that the floating effect can be suppressed considerably.

[0052]

The PDSOI-MOSFET having the above-mentioned structure according to the first embodiment has such a feature that the depletion layer 90 directly under the central "–" portion of the H gate electrode 71 does not reach the buried oxide film 2. Because of such a feature, the PDSOI-MOSFET has an excellent controllability of the threshold voltage.

[0053]

Therefore, the semiconductor device according to the first embodiment has the H gate electrode structure and is provided with the body regions 13, 13 in a region where

the PDSOI-MOSFET is to be formed. Consequently, it is possible to provide a stronger body potential than that in the conventional PDSOI-MOSFET shown in Figs. 1 and 2 and to fix the body potential having high stability. This respect will be described below in detail.

[0054]

In the conventional PDSOI-MOSFET shown in Figs. 1 and 2, the body terminals 25 and the channel region are electrically connected to each other through the thin p well region 11 directly under the partial isolation. Therefore, the body resistance is comparatively high and a transistor characteristic is prone to variations depending on a distance from the body terminals 25.

[0055]

On the other hand, in the structure according to the first embodiment, the body terminals 28 are provided on the body region 13 formed in the vicinity of the source region 51 and the drain region 61 in the PDSOI-MOSFET formation region in addition to the body terminals 25 on the body regions 10 provided with the partial isolation region (the partial oxide film 31 and the p well region 11 provided thereunder) therebetween. These two types of body terminals 25 and 28 can reduce the body resistance value and can effectively suppress variations in transistor characteristic.

[0056]

Moreover, the reduction in the body resistance can raise a drain breakdown voltage. To the contrary, in the case in which the thickness of the p well region 11 provided under the partial oxide film 31 is proportional to that of the SOI layer 4 and the same body resistance is set, the thickness of the SOI layer 4 can be reduced by employing the H gate electrode structure.

[0057]

When the thickness of the SOI layer 4 is reduced, there is a possibility that a junction capacitance of a line component (a longitudinal component) of the source/drain might be reduced, resulting in an increase in speed. Moreover, the use of the H gate electrode structure can reduce an edge leakage (edge parasitic MOS) resulting from the isolation. Furthermore, it is possible to prevent the reliability of the gate oxide film from being deteriorated due to the isolation edge. The edge leakage resulting from the isolation and the deterioration in the reliability of the gate oxide film will be described below in detail.

[0058]

The PDSOI-MOSFET according to the first embodiment having the above-mentioned features can be used particularly effectively for an I/O circuit, an analog circuit (a PLL, a sense amplifier circuit), a timing circuit, a dynamic circuit and the like in which the fixation of the body potential is greatly required.

[0059]

(Classification according to Source/Drain Regions)

(First Mode : a structure in which both the source region and the drain region are in direct contact with the buried oxide film 2 (the structure shown in Figs. 3 to 5))

As shown in Fig. 4, the source region 51 and the drain region 61 are in direct contact with the buried oxide film 2. Therefore, the effect of fixing the body potential through the body terminals 25 provided on the body regions 10 is reduced.

[0060]

According to the structure of the first mode, however, a pn junction is not formed on the bottom surfaces of the source region 51 and the drain region 61. Correspondingly, the area of a pn junction interface is reduced so that a junction leakage can be suppressed. Moreover, a junction capacitance can be reduced.

[0061]

(Second Mode : a structure in which the depletion layer extending from the source region and the drain region, as well as the source region and the drain region, are out of contact with the buried oxide film)

Fig. 6 is a sectional view showing a second mode of the first embodiment. Fig. 6 corresponds to a section taken along the line A2-A2 of Fig. 3.

[0062]

As shown in Fig. 6, a source region 52 and a drain region 62 do not reach the buried oxide film 2 but are formed in the SOI layer 4. Furthermore, a depletion layer 91 extending from the source region 52 and the drain region 62 during a normal operation does not reach the buried oxide film 2. Other structures are the same as those in the first mode.

[0063]

According to the second mode, the source region 52, the drain region 62, and the depletion layer 91 extending from the source region 52 and the drain region 62 do not reach the buried oxide film 2. This reduces a body resistance R1 from the body terminals 25 to the channel region, and provides an advantage that the effect of fixing the body potential through the body terminals 25 is the greatest. However, there is a disadvantage that the pn junction capacitance is increased.

[0064]

(Third Mode : a structure in which the drain region is out of contact with the buried oxide film but the depletion layer extending from the drain region is out of contact with the buried oxide film)

Fig. 7 is a sectional view showing a third mode of the first embodiment. Fig. 7 corresponds to the section taken along the line A2-A2 of Fig. 3.

[0065]

As shown in Fig. 7, a source region 53 and a drain region 63 do not reach the buried oxide film 2 but are formed in the SOI layer 4. However, a depletion layer 92 extending from the source region 53 and the drain region 63 during a normal operation reaches the buried oxide film 2. Other structures are the same as those in the first mode.

[0066]

In the third mode, since the drain region 63 is not in direct contact with the buried oxide film 2, the effect of fixing the body potential is therefore greater than that in the first mode. In addition, since the depletion layer 92 is in contact with the buried oxide film 2, the pn junction capacitance is also reduced. In the case in which the depletion layer 92 extending from the drain region 63 is in contact with the buried oxide film 2 at a voltage of 0 V, there is a greater advantage that the pn junction capacitance can be reduced. While the depletion layer 92 extending from the source region 53 is also in contact with the buried oxide film 2 in the example of Fig. 7, the same effects can be obtained even if it is not in contact with the buried oxide film 2.

[0067]

(Fourth Mode : an asymmetrical structure in which the drain region is deeper than the source region and the drain region or the depletion layer extending from the drain region is in contact with the buried oxide film)

Fig. 8 is a sectional view showing a fourth mode of the first embodiment. Fig. 8 corresponds to the section taken along the line A2-A2 of Fig. 3.

[0068]

As shown in Fig. 8, there is provided an asymmetrical source/drain structure in which, although the source region 52 and a depletion layer 94 extending from the source region 52 do not reach the buried oxide film 2, the drain region 61 is in direct contact with

the buried oxide film 2. Other structures are the same as those in the first mode.

[0069]

The asymmetrical source/drain structure can be fabricated by separately implanting ions into the source and the drain using a resist mask.

[0070]

In the fourth mode having such a structure, the junction capacitance of the source region 52 has little effect on the operating speed of the circuit. Therefore, even if the depletion layer 94 extending from the source region 52 is out of contact with the buried oxide film 2, there is no adverse effect. Since the depletion layer 94 extending from the source region 52 is out of contact with the buried oxide film 2, a body resistance value R1S provided under a region from a channel region to the vicinity of the source region 52 can be reduced. Moreover, while the source region may be formed with a structure in which the depletion layer 94 is in contact with the buried oxide film 2, it is more desirable that the depletion 94 should not reach the buried oxide film 2 because the area of the pn junction interface can be reduced.

[0071]

Since the drain region 61 is in contact with the buried oxide film 2, the junction capacitance and the area of the pn junction interface can be reduced. Furthermore, if the drain region 61 is out of contact with the buried oxide film 2 but the depletion layer extending from the drain region 61 during a normal operation is in contact with the buried oxide film 2, the body resistance value can be reduced.

[0072]

<Second Embodiment>

Fig. 9 is a plan view showing a planar structure of a semiconductor device according to a second embodiment of the present invention. A section taken along the

line A3-A3 of Fig. 9 is the same as the shape shown in Fig. 4, and a section taken along the line B1-B1 of Fig. 9 is the same as the shape shown in Fig. 5 except that the body region 13 is formed on one of sides.

[0073]

As shown in Fig. 9, a PDSOI-MOSFET according to the second embodiment has a structure in which a T gate electrode 72 is employed in place of the H gate electrode 71 of the first embodiment. More specifically, while the body regions 13 are formed near the left and right "I"s of the H gate electrode 71 according to the first embodiment, the body region 13 is formed near the single "I" of the T gate electrode 72 in the same manner as the H gate electrode 71 according to the second embodiment. Since other structures are the same as those in the first embodiment, description thereon will be omitted.

[0074]

In the T gate electrode 72 according to the second embodiment, body fixation is carried out by the body terminals 25 and 28 provided on the body regions 10 and 13 of two types in the same manner as in the first embodiment. Consequently, the body resistance value can be reduced and variations in transistor characteristic can be suppressed effectively.

[0075]

In the T gate electrode 72 according to the second embodiment, an area covering an edge of an active region (the source region 51, the drain region 61 or the like where the partial oxide film 31 is not formed) can be reduced. Therefore, the gate capacitance can be reduced below that of the H gate electrode 71. Consequently, the operation of the circuit can be carried out more quickly than that of the PDSOI-MOSFET according to the first embodiment.

[0076]

Moreover, the problem of the isolation edge is also effective in the second embodiment having the T gate electrode 72 in the same manner as that in the first embodiment.

[0077]

Accordingly, the PDSOI-MOSFET according to the second embodiment can be used particularly effectively for an I/O circuit, an analog circuit (a PLL, a sense amplifier circuit), a timing circuit, a dynamic circuit and the like in which the fixation of a body potential is greatly required.

[0078]

The structure according to the second embodiment is classified into first to fourth modes depending on the junction position of the source/drain regions in the same manner as that in the first embodiment.

[0079]

<Third Embodiment>

Fig. 10 is a plan view showing a planar structure of a semiconductor device according to a third embodiment of the present invention, Fig. 11 is a sectional view showing a section taken along the line A4-A4 of Fig. 10, and Fig. 12 is a sectional view showing a section taken along the line A5-A5 of Fig. 11.

[0080]

As shown in these drawings, the source region according to the third embodiment presents a source-tied structure in which a p^+ region 55 (a body-fixing semiconductor region) is provided between two separate portions of a source region 54.

[0081]

Moreover, the source region 54, the p^+ region 55 and the drain region 61 are

formed to have such depths as to reach the back face of the SOI layer 4 from the surface thereof.

[0082]

The gate oxide film 5 is formed on the SOI layer 4 between the source region 54 (p^+ region 55) and the drain region 61, and the gate electrode 7 is formed on the gate oxide film 5. The side walls 6 are formed on side surfaces of the gate electrode 7.

[0083]

The body regions 10 are isolated by the partial oxide film 31 and the p well region 11 provided thereunder and are formed to extend from the surface of the SOI layer 4 to the back face thereof. The body regions 10 are electrically connected to the body region main part which is part of the SOI layer 4 provided under the gate electrode 7 through the p well region 11 provided under the partial oxide film 31.

[0084]

Such a source-tied structure in the PDSOI-MOSFET according to the third embodiment can fix the electric potentials of the source and the body simultaneously in a source junction region as shown in Figs. 10, 11 and 12. More specifically, part of the source region acts as the p^+ region 55. Therefore, the source region 54 and the p^+ region 55 are set to have the same electric potential so that the body potential can be fixed with high stability. As a matter of course, the body potential can also be fixed by the body regions 10.

[0085]

Accordingly, the PDSOI-MOSFET according to the third embodiment having the above-mentioned features can be used particularly effectively for an I/O circuit, an analog circuit (a PLL, a sense amplifier circuit), a timing circuit, a dynamic circuit and the like in which the fixation of the body potential is greatly required.

[0086]

Moreover, the structure according to the third embodiment is classified into a first mode to a fourth mode depending on the junction position of the source/drain regions in the same manner as that in the first embodiment.

[0087]

<Fourth Embodiment>

Fig. 13 is a plan view showing a planar structure of a semiconductor device according to a first mode of a fourth embodiment of the present invention. A section taken along the line A6-A6 of Fig. 13 is the same as the shape shown in Fig. 11, a section taken along the line A7-A7 of Fig. 13 is the same as the shape shown in Fig. 12, and a section taken along the line B3-B3 of Fig. 13 is the same as the shape shown in Fig. 5.

[0088]

The structure according to a first mode of the fourth embodiment is a combination of the H gate electrode 71 according to the first embodiment and the source-tied structure according to the third embodiment. Combination of the body potential fixation according to the first and third embodiments (the body potential fixation by means of the body regions 10, the two body regions 13 and the p^+ region 55) further enhances the body potential fixation.

[0089]

Fig. 14 is a plan view showing a planar structure of a semiconductor device according to a second mode of a fourth embodiment of the present invention. A section taken along the line A8-A8 of Fig. 14 is the same as the shape shown in Fig. 11, and a section taken along the line A9-A9 of Fig. 14 is the same as the shape shown in Fig. 12.

[0090]

The structure according to the second mode of the fourth embodiment is a

combination of the T gate electrode 72 according to the second embodiment and the source-tied structure according to the third embodiment. Combination of the body potential fixation according to the second and third embodiments (the body potential fixation by means of the body regions 10, the single body region 13 and the p^+ region 55) further enhances the body potential fixation.

[0091]

Fig. 15 is a plan view showing a planar structure of a semiconductor device according to a third mode of the fourth embodiment of the present invention. A section taken along the line A10-A10 of Fig. 15 is the same as the shape shown in Fig. 11, a section taken along the line A11-A11 of Fig. 15 is the same as the shape shown in Fig. 12, and a section taken along the line B4-B4 of Fig. 15 is the same as the shape shown in Fig. 5.

[0092]

The structure according to the third mode of the fourth embodiment is a combination of a special H gate electrode 73 obtained by improving the H gate electrode 71 according to the first embodiment and the source-tied structure according to the third embodiment. Combination of the body potential fixation according to the first and third embodiments further enhances the body potential fixation.

[0093]

In the third mode according to the fourth embodiment, the source region 54 and the p^+ region 55 are isolated by isolating portions 73a of the special H gate electrode 73.

[0094]

The gate electrode according to the third embodiment and the first and second modes of the fourth embodiment does not have a portion corresponding to the isolating portions 73a. Therefore, when a silicide region is formed on the source region 54, the

source region 54 and the p^+ region 55 are short-circuited. For this reason, the source and the drain cannot be utilized with their functions reversed.

[0095]

On the other hand, in the third mode according to the fourth embodiment, the presence of the isolating portions 73a prevents the short-circuit between the source region 54 and the p^+ region 55 even if the silicide region is formed on the source region 54. This allows the use of the source and the drain with their functions reversed. However, a gate capacitance is increased corresponding to the presence of the isolating portions 73a. Thus, the operation speed is lower than that in the first mode. A p^- body region is formed under the isolating portions 73a, with an oxide film therebetween.

[0096]

Accordingly, the PDSOI-MOSFET according to the first to third modes of the fourth embodiment described above can be used particularly effectively for an I/O circuit, an analog circuit (a PLL, a sense amplifier circuit), a timing circuit, a dynamic circuit and the like in which the fixation of the body potential is greatly required.

[0097]

Moreover, the structure according to the fourth embodiment is classified into the first mode to the fourth mode depending on the junction position of the source/drain regions in the same manner as that in the first embodiment.

[0098]

<Fifth Embodiment>

While the semiconductor device has the single PDSOI-MOSFET isolated by the partial isolation region in each of the first to fourth embodiments, a semiconductor device according to a fifth embodiment has plural types of PDSOI-MOSFETs isolated by the partial isolation region. The types of the PDSOI-MOSFETs are as follows:

Type 1 : The body potential is fixed with the normal gate structure (see Figs. 1 and 2).

Type 2 : The body potential is fixed with the H gate electrode structure (the first embodiment).

Type 3 : The body potential is fixed with the T gate electrode structure (the second embodiment).

Type 4 : The body potential is fixed with the source-tied structure (the third embodiment).

In some cases, the type 4 and the type 2 or the type 3 are combined (the fourth embodiment).

[0099]

(Body Floating Type)

Fig. 16 is a plan view showing a planar structure of a type 5 (No. 1) of the PDSOI-MOSFET. As shown in Fig. 16, the body region main part of the PDSOI-MOSFET is also brought into a floating state in the absence of the body regions 10 and the body terminals 25.

[0100]

Fig. 17 is a plan view showing a planar structure of the type 5 (No. 2) of the PDSOI-MOSFET. As shown in Fig. 17, the body region of the PDSOI-MOSFET is brought into the floating state with such a structure that the potential fixation is not carried out by the body terminal even if the body region 10 is provided.

[0101]

Thus, such a type as to bring the body region into the floating state is classified as a new type. The PDSOI-MOSFET of the type 5 can produce the effect of setting the threshold voltage at a lower level than that of the types 1 to 4 in which the body potential

is fixed.

[0102]

In such a body floating type, the normal electrode structure such as the gate electrode 7 is classified as the type 5, and such types as to make the body floating with the H gate electrode structure and the T gate electrode structure in place of the gate electrode 7 in the same manner as the types 2 and 3 are classified as types 6 and 7, respectively. In the types 6 and 7, it is a matter of course that the body potential fixation is not carried out by the body terminal(s) 28 provided on the body region(s) 13.

[0103]

The floating types of the PDSOI-MOSFETs will be listed below.

[0104]

Type 5: The body is made floating with the normal gate structure (a linked-body structure in which the body regions 10 shown in Fig. 15 are not usually provided).

Type 6: The body is made floating with the H gate electrode structure.

Type 7: The body is made floating with the T gate electrode structure.

The body region size has the following relationship: the type 6 > the type 7 > the type 5. Therefore, if other conditions are identical, the threshold voltage has the following relationship: the type 5 < the type 7 < the type 6, depending on the easiness to cause carriers to escape into the body region.

[0105]

The semiconductor device according to the fifth embodiment is such that the PDSOI-MOSFETs of at least two of the types 1 to 7 are formed in at least two element formation regions isolated by a partial isolation region.

[0106]

In the semiconductor device according to the fifth embodiment having such a structure, plural types of PDSOI-MOSFETs differing from each other in at least one of the body region structure, the gate electrode structure and the presence/absence of the body potential fixation thereby to have different transistor characteristics such as threshold voltage can be provided in a plurality of element formation regions isolated by the partial isolation region.

[0107]

As a result, it is possible to constitute a semiconductor integrated circuit having a high function by using the PDSOI-MOSFETs according to the transistor characteristic among those of the plural types.

[0108]

Furthermore, it is possible to set the threshold voltages of the respective PDSOI-MOSFETs at different values by changing a channel concentration, the thickness of the SOI layer 4, the thickness and material of the gate oxide film 5 and the like in each of the PDSOI-MOSFETs.

[0109]

Moreover, it is also possible to provide the PDSOI-MOSFETs having different threshold voltages by using the PDSOI-MOSFETs of at least two of the types 1 to 4 and by setting the substrate biases (body potential fixing voltages) thereof at different levels.

[0110]

<Sixth Embodiment>

A semiconductor device according to a sixth embodiment is of a partial isolation and complete isolation combination type having a first element formation region isolated by the partial isolation region, and a second element formation region isolated by a complete isolation region (an insulation film for isolation reaching the back face (the

buried oxide film 2) of the SOI layer 4 from the surface thereof).

[0111]

The types of the PDSOI-MOSFETs isolated by the complete isolation region will be listed below.

[0112]

Fig. 18 is a sectional view showing a sectional structure of a PDSOI-MOSFET of a type A. As shown in Fig. 18, the PDSOI-MOSFET is formed in a region isolated by a complete oxide film 32 serving as the complete isolation region provided to reach the back face (the buried oxide film 2) of the SOI layer 4 from the surface thereof. The structure is the same as the planar structure according to the first embodiment shown in Fig. 4 except that the partial oxide film 31 is replaced with the complete oxide film 32 and the body region 10 and the body region 25 are not present.

[0113]

Fig. 19 is a plan view showing a planar structure of the PDSOI-MOSFET of the type A. A section taken along the line A12-A12 of Fig. 19 corresponds to Fig. 18.

[0114]

As shown in Fig. 19, the planar structure is the same as the planar structure according to the first embodiment shown in Fig. 4 except that the partial oxide film 31 is replaced with the complete oxide film 32 and the body region 10 is not present.

[0115]

In the PDSOI-MOSFET of the type A, the body potential fixation is carried out by the two body terminals 28 provided on the two body regions 13. Consequently, the body resistance value can be reduced and the variations in transistor characteristic can be suppressed effectively. Unlike the first embodiment, however, it is impossible to carry out the body potential fixation by means of the body terminals 25 provided on the body

regions 10.

[0116]

Fig. 20 is a plan view showing a planar structure of a PDSOI-MOSFET of a type B. As shown in Fig. 20, the planar structure is the same as the planar structure according to the second embodiment except that the partial oxide film 31 is replaced with the complete oxide film 32 and the body region 10 is not present. A section taken along the line A13-A13 of Fig. 20 is the same as the sectional structure shown in Fig. 18.

[0117]

In the PDSOI-MOSFET of the type B, the body potential fixation is carried out by the body terminal 28 provided on the single body region 13. Consequently, the body resistance value can be reduced and the variations in transistor characteristic can be suppressed effectively. Unlike the second embodiment, however, it is impossible to carry out the body potential fixation by means of the body terminal 25 provided on the body region 10.

[0118]

A type C is such that the body potential fixation is carried out with the source-tied structure in the complete isolation region, as in the third embodiment.

[0119]

Fig. 21 is a plan view showing a planar structure of a PDSOI-MOSFET of a type D. As shown in Fig. 21, this PDSOI-MOSFET is the same as the PDSOI-MOSFET of the type 5 which is partially isolated as shown in Fig. 16 except that the partial oxide film 31 is replaced with the complete oxide film 32. A section taken along the line A14-A14 of Fig. 21 is the same as the sectional structure shown in Fig. 18.

[0120]

Similarly, there are types E and F similar to the PDSOI-MOSFETs of the types

6 and 7 except that the partial oxide film 31 is replaced with the complete oxide film 32.

[0121]

In the case in which other conditions are identical for the same reasons as the types 5 to 7, the threshold voltage has the following relationship: the type D < the type F < the type E.

[0122]

As described above, the types A to F are the types of the PDSOI-MOSFET formed in the second region isolated by the complete isolation region. The above-mentioned types A to F can be summarized as follows.

[0123]

Type A: The body potential is fixed with the H gate electrode structure (which is similar to that in the first embodiment, but the body potential fixation is not carried out by the body regions 10).

Type B: The body potential is fixed with the T gate electrode structure (which is similar to that in the second embodiment, by the body potential fixation is not carried out by the body regions 10).

Type C: The body potential is fixed with the source-tied structure (which is similar to that in the third embodiment, but the body potential fixation is not carried out by the p^+ region 55).

Type D: The body is made floating with the normal gate structure.

Type E: The body is made floating with the H gate electrode structure.

Type F: The body is made floating with the T gate electrode structure.

[0124]

The PDSOI-MOSFETs of the types A to F are formed in the second element formation region isolated by the complete isolation region, thereby to produce the effect

of being latchup free.

[0125]

The use of the H gate electrode structure and the T gate electrode structure as in the types A and B or the use of the source-tied structure as in the type C accomplishes the body potential fixation to suppress the floating-body effect.

[0126]

On the other hand, the types of the PDSOI-MOSFETs formed in the first element formation region isolated by the partial isolation region are the types 1 to 7 described in the fifth embodiment.

[0127]

In the case in which other conditions are identical, the threshold voltages of the PDSOI-MOSFETs have the following relationship: "the complete isolation floating structure (the types D to F) < the partial isolation floating structure (the types 5 to 7) < the body potential fixing structure (the type A, the type B, and the types 1 to 4).

[0128]

The threshold voltage in the partial isolation floating structure is greater than that in the complete isolation floating structure. This is because the partial isolation floating structure having the body region greater than that in the complete isolation floating structure produces the higher effect of causing carriers (holes in an NMOS and electrons in a PMOS) to disappear which give rise to the floating-body effect.

[0129]

The semiconductor device according to the sixth embodiment has the partial isolation and complete isolation combination structure in which the PDSOI-MOSFET of at least one of the types 1 to 7 described above is formed in the first element formation region isolated by the partial isolation region and the PDSOI-MOSFET of at least one of

the types A to F is formed in the second element formation region isolated by the complete isolation region.

[0130]

The semiconductor device according to the sixth embodiment having such a structure comprises plural types of PDSOI-MOSFETs. Therefore, it is possible to provide the PDSOI-MOSFETs applicable to respective uses.

[0131]

It is possible to set the threshold voltages of the respective PDSOI-MOSFETs of plural types at different levels by changing the channel concentration, the thickness of the SOI layer 4, the thickness and material of the gate oxide film 5 and the like in each of the plural types of PDSOI-MOSFETs.

[0132]

Moreover, it is also possible to provide the PDSOI-MOSFETs having different threshold voltages by using the PDSOI-MOSFETs of at least two of the types 1 to 4 and by setting the substrate biases (body potential fixing voltages) thereof at different levels.

[0133]

Fig. 22 is a view conceptually showing a planar structure of the semiconductor device according to the sixth embodiment. As shown in Fig. 22, the structure includes partial isolation regions 131 (131A to 131G) isolated by the partial oxide film 31 and a complete isolation region 132 isolated by the complete oxide film 32. In the example of Fig. 22, the PDSOI-MOSFETs of the body potential fixing types 1 to 4 are provided in the partial isolation region 131B, the PDSOI-MOSFETs of the type A, the type B and the types D to F are provided in the complete isolation region 132, the body floating type PDSOI-MOSFET of the type 5 is provided in the partial isolation region 131D, and the body floating type PDSOI-MOSFETs of the types 6 and 7 are provided in the partial

isolation region 131E.

[0134]

(First Application)

Fig. 23 is a circuit diagram showing a first application of the semiconductor device according to the sixth embodiment. As shown in Fig. 23, a 3-input NAND gate (a semiconductor integrated circuit) is constituted by PMOS transistors Q11 to Q13 and NMOS transistors Q21 to Q23B.

[0135]

The NMOS transistors Q21 to Q23 are connected in series in this order between a node N1 and a ground, and the PMOS transistors Q11 to Q13 are connected in parallel between an output terminal 33 and the node N1. An input signal IN1 is input to the gates of the PMOS transistor Q11 and the NMOS transistor Q21, an input signal IN2 is input to the gates of the PMOS transistor Q12 and the NMOS transistor Q22, and an input signal IN3 is input to the gates of the PMOS transistor Q13 and the NMOS transistor Q23.

[0136]

With such a structure, the complete isolation floating structure (for example, the type D) is used for the NMOS transistor Q21, the linked-body structure (the type 5) having the partial isolation floating structure and having neither the body region nor the body terminal is used for the NMOS transistor Q22, and the partial isolation body potential fixing structure (any one of the types 1 to 4) is used for the NMOS transistor Q23.

[0137]

Thus, the plural kinds of PDSOI-MOSFETs are used properly for the NMOS transistors Q21 to Q23, and are arranged so that the NMOS transistors Q21 to Q23 are in

increasing order of substrate bias effect.

[0138]

More specifically, it is possible to effectively suppress the reduction in speed due to the substrate bias effect by using MOS transistors having such a character as to be influenced by the substrate bias effect in the order of Q21 to Q23 as the NMOS transistors Q21 to Q23 placed in such a situation as to be influenced by the substrate bias effect in the order of Q21 to Q23.

[0139]

(Second Application)

Fig. 24 is a circuit diagram showing a second application of the semiconductor device according to the sixth embodiment. A shown in Fig. 24, a plurality of inverters IV are connected in series to implement an inverter chain (or a ring oscillator).

[0140]

Each inverter IV is constituted by a PMOS transistor Q15 and an NMOS transistor Q25. The PMOS transistors Q15 have respective drains connected to a node N2 in common, and the node N2 is connected to a power supply voltage VDD through a PMOS transistor Q14. A control signal S14 is applied to the gate of the PMOS transistor Q14. The NMOS transistors Q25 have respective sources grounded in common.

[0141]

When the PMOS transistor Q14 is OFF, each inverter IV is brought into an inactive state. When the PMOS transistor Q14 is ON, each inverter IV is brought into an active state.

[0142]

With such a structure, the complete isolation floating structure (the types D to

F) or a partial isolation linked-body structure (the type 5) is used for the PMOS transistor Q15 and the NMOS transistor Q25 which constitute the inverter IV. These structures can set a threshold voltage at a level lower than that in the body potential fixing structure. Therefore, the inverter IV can be operated at a high speed.

[0143]

On the other hand, it is possible to increase the threshold voltage by using the partial isolation body potential fixing structure (the types 1 to 4) for the PMOS transistor Q14 for switching control of the inverter IV. This reduces power consumption in the power-OFF state.

[0144]

Thus, it is possible to increase the speed and to reduce the power consumption by properly using plural types of PDSOI-MOSFETs for the MOS transistors Q15 and Q25 constituting the inverter IV and the PMOS transistor Q14 and by changing the threshold voltages thereof.

[0145]

(Supplement)

Fig. 25 is a sectional view showing a structure of an FD (Fully-Depleted) SOI-MOSFET structure isolated by a complete isolation region. As shown in Fig. 25, an apparent structure is the same as the complete isolation body floating structure shown in Fig. 16.

[0146]

The FDSOI-MOSFET is different from the PDSOI-MOSFET in that the depletion layer 94 directly under the gate electrode 7 reaches the buried oxide film 2. The FDSOI-MOSFET may have such a structure that an n^- region of the source/drain reaches the buried oxide film 2.

[0147]

The FDSOI-MOSFET shown in Fig. 25 may be of any one of the types A to F of the complete isolation structure or any one of the types 1 to 7 of the partial isolation structure.

[0148]

The FDSOI-MOSFET has an advantage that a subthreshold coefficient is good, that is, a switching speed is good. However, there is also a disadvantage in threshold variations due to variations in thickness of the SOI layer 4. In this respect, the PDSOI-MOSFET has a high controllability of the threshold voltage because the depletion layer directly under the gate is out of contact with the buried oxide film.

[0149]

It is also possible to further diversify the types of transistors to be used by adding the FDSOI-MOSFET shown in Fig. 25 to the types of transistors used in the fifth embodiment or the sixth embodiment.

[0150]

While the structure of the NMOS transistor has mainly been described in the first to sixth embodiments, it is apparent that the present invention can also be applied to a PMOS transistor and a CMOS transistor.

[0151]

<Seventh Embodiment>

(First Mode)

Fig. 26 is a sectional view showing a resistive element of a semiconductor device according to a first mode of a seventh embodiment of the present invention, and Fig. 27 is a plan view. A section taken along the line C1-C1 of Fig. 27 corresponds to Fig. 26.

[0152]

As shown in these drawings, p^+ regions 21 and 22 are isolated by a partial oxide film 31a and the p well region 11 provided thereunder. The p^+ region 21 and the p^+ region 22 are electrically connected to each other through the p well region 11 provided under the partial oxide film 31a, and a resistive element R3 can be formed between a resistive terminal 23 provided on the p^+ region 21 and a resistive terminal 24 provided on the p^+ region 22.

[0153]

More specifically, the resistive element R3 is formed by using the p well region 111 which is part of the SOI layer 4 provided under the partial oxide film 31a. The resistance value of the resistive element R3 can be controlled based on the thickness of the partial oxide film 31a (that is, the thickness of the p well region 11 provided under the partial oxide film 31a).

[0154]

The outer periphery of the resistive element R3 is isolated by the partial oxide film 31 which is different from the partial oxide film 31a. An n well region 12 and an n^+ guard ring region 20 are formed. The n^+ guard ring region 20 is selectively formed in the n well region 12. A resistive element formation region where the resistive element R3 is formed is isolated from other elements by the n^+ guard ring region 20 and the n well region 12.

[0155]

Fig. 28 is a sectional view showing a general resistive element. As shown in Fig. 28, the p^+ regions 21 and 22 are selectively provided in an upper portion of the p well region 11. The p^+ region 21 and the p^+ region 22 are electrically connected to each other through the p well region 11. Consequently, the resistive element R3 is formed between

the resistive terminal 23 provided on the p^+ region 21 and the resistive terminal 24 provided on the p^+ region 22. Other structures are the same as those in the first mode.

[0156]

According to the first mode shown in Fig. 23, the p well region 11 provided under the partial oxide film 31 is utilized to form a resistor. This increases the resistance value of the general resistive element shown in Fig. 28.

[0157]

(Second Mode)

Fig. 29 is a sectional view showing a resistive element of a semiconductor device according to a second mode of the seventh embodiment. The second mode employs a partial isolation and complete isolation combination structure.

[0158]

As shown in Fig. 29, the resistive element R3 is formed in the p well region 11 provided under the partial oxide film 31 between the resistive terminal 23 provided on the p^+ region 21 and the resistive terminal 24 provided on the p^+ region 22 in the same manner as that in the first mode.

[0159]

The resistive element R3 is completely isolated from its surroundings by the complete oxide film 32. Therefore, it is not necessary to provide the n well region 12 and the n^+ guard ring region 20 which have been provided in the first mode.

[0160]

(Third Mode)

Fig. 30 is a sectional view showing a resistive element formation region of a semiconductor device according to a third mode of the seventh embodiment.

[0161]

As shown in Fig. 30, the p^+ regions 21 and 22 are isolated by the partial isolation region including the partial oxide film 31 and the p well region 11 provided thereunder. The p^+ region 21 and the p^+ region 22 are electrically connected to each other through the p well region 11 provided under two partial oxide films 31a and a p well region 11a where the partial oxide film 31 is not formed, and a resistive element R34 can be formed between the resistive terminal 23 provided on the p^+ region 21 and the resistive terminal 24 provided on the p^+ region 22. Other structures are the same as those in the first mode.

[0162]

According to the third mode, the resistive element R34 is formed by the p well region 11a on which the partial oxide film 31 is not formed. Therefore, the dishing problem can be suppressed during the formation of the partial oxide film 31.

[0163]

In the seventh embodiment described above, impurities which determine a resistance value are implanted through the partial oxide film 31 during the formation of the source/drain regions. Therefore, it is possible to suppress variations in resistance value by the provision of the region where the partial oxide film 31 is not formed as in the third mode.

[0164]

(Application)

Fig. 31 is a circuit diagram showing an SRAM cell having a 6-transistor CMOS structure. As shown in Fig. 31, a CMOS inverter having an NMOS transistor Q1 and a PMOS transistor Q5 and a CMOS inverter having an NMOS transistor Q2 and a PMOS transistor Q6 are cross-connected between nodes N11 and N12, thereby to form a latch.

[0165]

An NMOS transistor Q3 is inserted between a bit line BL1 and the node N11, and an NMOS transistor Q4 is inserted between a bit line BL2 and the node N12. The gates of the NMOS transistors Q3 and Q4 are connected to a word line WL. The NMOS transistors Q1 and Q2 and the PMOS transistors Q5 and Q6 are referred to as driver transistors, and the NMOS transistors Q3 and Q4 are referred to as access transistors.

[0166]

Fig. 32 is a plan view showing a layout structure for implementing the SRAM cell illustrated in Fig. 31. As shown in Fig. 32, active regions 66 to 69 isolated by the partial oxide film 31 are selectively formed. The active regions 66 and 69 are n-type impurity regions and the active regions 67 and 68 are p-type impurity regions.

[0167]

In Fig. 32, a gate electrode 78 is formed over and extends across the active region 66, a gate electrode 79 is formed over and extends across the active regions 66 and 67, a gate electrode 80 is formed over and extends across the active regions 68 and 69, and a gate electrode 81 is formed over and extends across the active region 69.

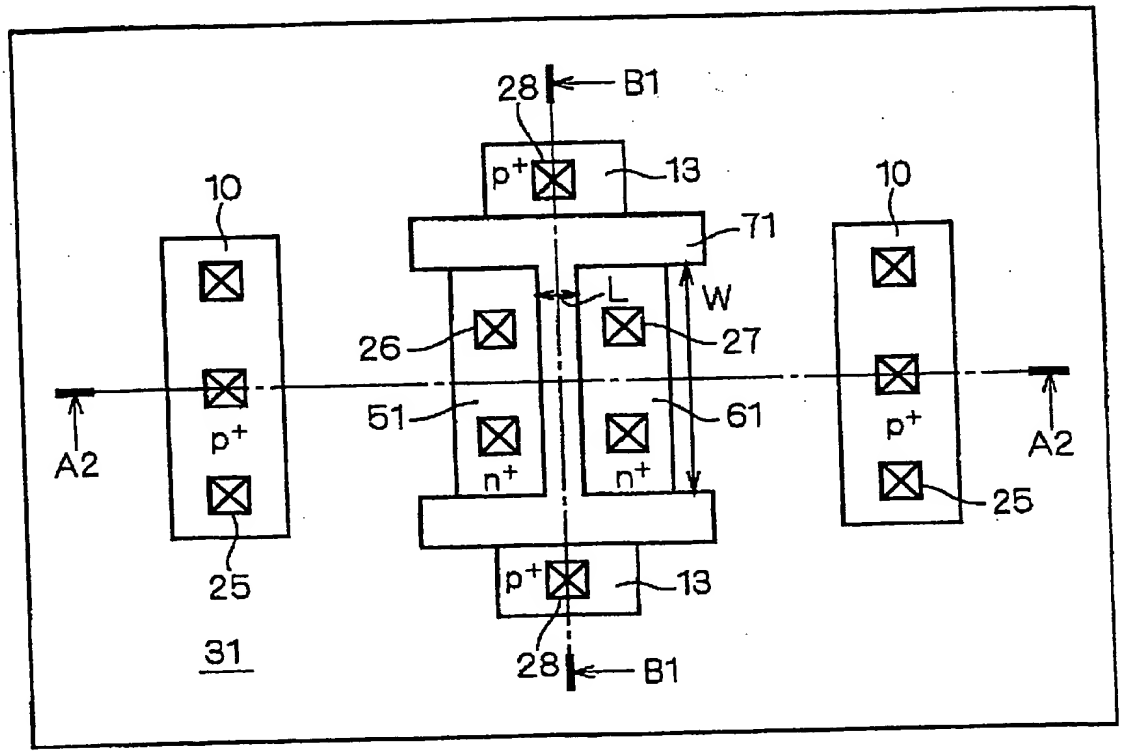
[0168]

The active regions 66 to 69 and the gate electrodes 78 and 82 are provided with contacts 76 in predetermined locations, and are electrically connected through the contacts 76 to interconnect lines such as a bit line BL and the word line WL not shown. The active region 67 is electrically connected to the gate electrode 80 through a shared contact 77. The active region 68 is electrically connected to the gate electrode 79 through a shared contact 77.

[0169]

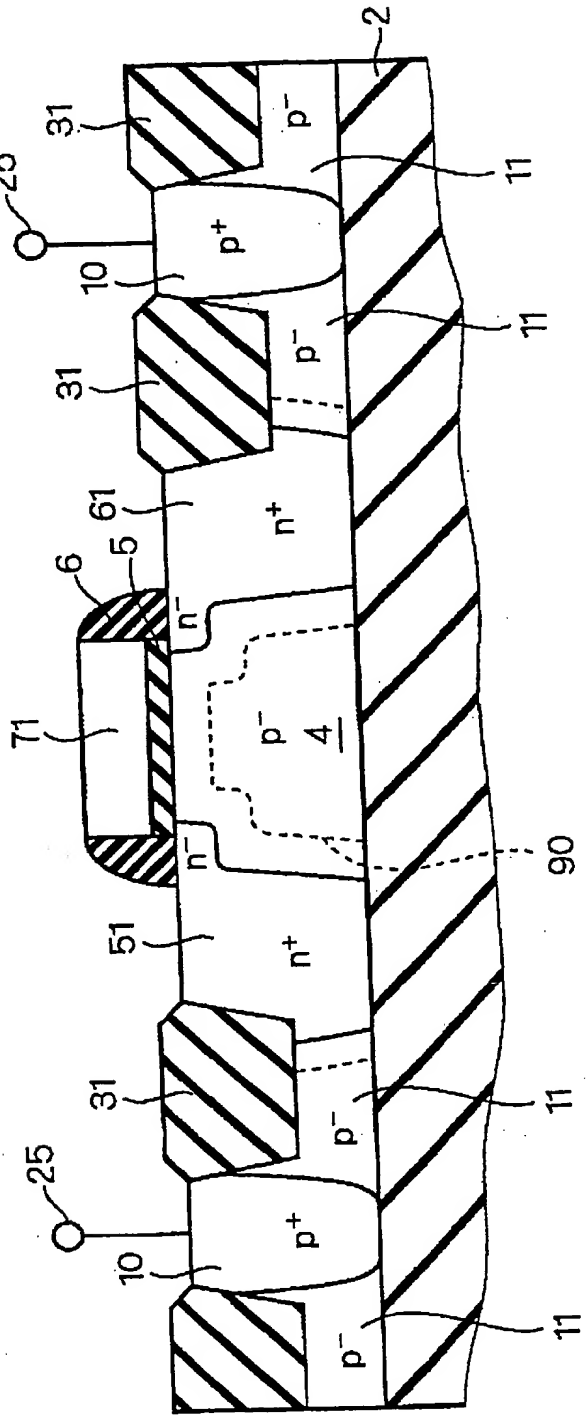
With such a structure, the NMOS transistor Q1 is constituted by the active region 66 and the gate electrode 79, the NMOS transistor Q2 is constituted by the active

[FIG. 3]

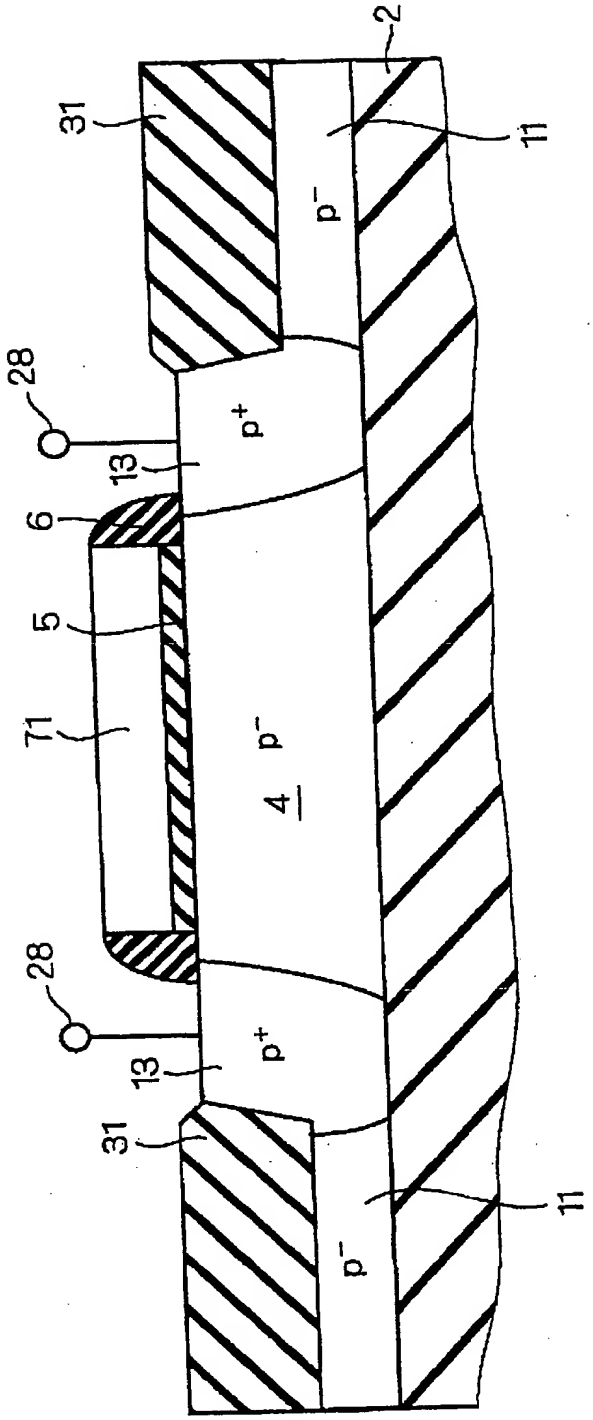


13: BODY REGION
71: H GATE ELECTRODE

[FIG. 4]



[FIG. 5]



region 69 and the gate electrode 80, the NMOS transistor Q3 is constituted by the active region 66 and the gate electrode 78, the NMOS transistor Q4 is constituted by the active region 69 and the gate electrode 81, the PMOS transistor Q5 is constituted by the active region 67 and the gate electrode 79, and the PMOS transistor Q6 is constituted by the active region 68 and the gate electrode 80.

[0170]

Fig. 33 is a circuit diagram showing an SRAM cell having a high resistance load type cell structure. As shown in Fig. 33, an NMOS inverter having the NMOS transistor Q1 and a resistor R11 and an NMOS inverter having the NMOS transistor Q2 and a resistor R12 are cross-connected between the nodes N11 and N12, thereby to form a latch. Other structures are the same as those of the SRAM cell shown in Fig. 31.

[0171]

Fig. 34 is a plan view showing a layout structure for implementing the SRAM cell illustrated in Fig. 33. As shown in Fig. 34, the active regions 66 and 69 isolated by the partial oxide film 31 are selectively formed. The active regions 66 and 69 are n-type impurity regions.

[0172]

Furthermore, p^+ regions 21a, 21b, 22a and 22b are selectively formed, and resistive layer formation well regions 82a and 82b where a resistive element shown in the second mode of the seventh embodiment is to be formed are provided between the p^+ regions 21a and 22a and the p^+ regions 21b and 22b, respectively. The resistive element formation well regions 82a and p^+ regions 21a and 22a, and the resistive element formation well region 82b and p^+ regions 21b and 22b are completely isolated from other elements by the complete oxide film 32 formed therearound.

[0173]

In Fig. 34, the gate electrode 78 is formed over and extends across the active region 66, the gate electrode 79 is formed over and extends across an active region 667, the gate electrode 80 is formed over and extends across the active region 69, and the gate electrode 81 is formed over and extends across the active region 69.

[0174]

The active regions 66 and 69 and the gate electrodes 78 to 82 are provided with the contacts 76 in predetermined locations, and are electrically connected through the contacts 76 to interconnect lines such as the bit line BL and the word line WL not shown. The p^+ region 22a is electrically connected to the gate electrode 80 through the shared contact 77, and the p^+ region 22b is electrically connected to the gate electrode 79 through the shared contact 77.

[0175]

With such a structure, the NMOS transistor Q1 is constituted by the active region 66 and the gate electrode 79, the NMOS transistor Q2 is constituted by the active region 69 and the gate electrode 80, the NMOS transistor Q3 is constituted by the active region 66 and the gate electrode 78, the NMOS transistor Q4 is constituted by the active region 69 and the gate electrode 81, the resistor R11 serving as a load resistor (LOAD element) is constituted by the p^+ regions 21a and 22a and the resistive element formation well region 82a, and the resistor R12 serving as the load resistor is constituted by the p^+ regions 21b and 22b and the resistive element formation well region 82b.

[0176]

A comparison between Fig. 32 and Fig. 34 shows that making the formation area of the resistive element formation well regions 82a and 82b smaller than that of the active regions 67 and 68 reduces the area of the SRAM cell.

[0177]

<Eighth Embodiment>

Fig. 35 is a plan view showing a general H gate electrode. As shown in Fig. 35, the H gate electrode 71 has left and right "I"s electrically isolating the body regions 16 adjacent in the gate width W direction to a source region 50 and a drain region 60 from the drain region 60 and the source region 50, and a central "–" functioning as the gate electrode of an original MOS transistor.

[0178]

With such a structure, p^+ implantation mask openings 15 for implantation into body regions 16 overlap end portions of the H gate electrode 71. This causes the end portions of the H gate electrode 71 to be implanted with p-type impurities in addition to n-type impurities, to present a problem in that the gate oxide film provided under the H gate electrode 71 is greatly damaged during the ion implantation. Moreover, there is a problem in that B, BF2 or the like implanted as the p-type impurities is diffused into a gate electrode region formed in an active region, resulting in variations in threshold voltage, depending on a process temperature.

[0179]

Fig. 36 is a plan view showing a planar structure of a semiconductor device according to an eighth embodiment of the present invention. Fig. 37 is a sectional view showing a section taken along the line D1-D1 of Fig. 36.

[0180]

As shown in these drawings, the H gate electrode 71 is provided with p^- body regions 17b adjacent to the left and right "I"s, and p^+ body regions 17a adjacent to the p^- body regions 17b to constitute body regions 17.

[0181]

Thus, the p^+ body regions 17a are spaced a distance r1 apart from the H gate

electrode 71 so that the p^+ implantation mask openings 16 are reliably prevented from overlapping the end portions of the H gate electrode 71.

[0182]

As compared with the structure shown in Fig. 35, this structure greatly reduces the damages to the gate oxide film provided under the H gate electrode 71 during the impurity implantation. This improves the reliability of the gate oxide film to effectively suppress the variations in threshold voltage.

[0183]

In addition, the distance r1 between the p^+ body regions 17a and the H gate electrode 71 prevents the threshold voltage from being varied due to the diffusion, into the gate electrode region, of B, BF2 or the like implanted as the p-type impurities for forming the p^+ body regions 17a.

[0184]

With the structure shown in Fig. 36, the p-type impurities are implanted into the end portions of the H gate electrode 71 during the formation of a pocket region at most. Therefore, the p-type impurity concentration in the end portions of the H gate electrode 71 can be reduced to 5×10^{18} cm^{-3} or less. Thus, the variations in threshold voltage can be suppressed.

[0185]

As shown in Fig. 37, the p^- body region 17b having a low impurity concentration is provided between the SOI layer 4 provided under the H gate electrode 71 and the p^+ body region 17a. Therefore, there is apprehension that a body resistance value might increase.

[0186]

However, the provision of silicide on the p^- body region 17b can solve the

problem comparatively easily. It is apparent that the eighth embodiment can be exactly applied to the T gate electrode structure as well as the H gate electrode structure.

[0187]

As to the isolation technique, the eighth embodiment is used for an H gate electrode and T gate electrode structure fabricated using the complete isolation, the partial isolation, and the partial isolation and complete isolation combination. It is apparent that this structure can also be applied to PMOS and CMOS.

[0188]

While the SOI transistor fabricated on single crystal Si has been described in the first to eighth embodiments, it is a matter of course that the present invention can also be applied to a polysilicon TFT (Thin Film Transistor) formed on polycrystalline Si.

[0189]

<Partial Isolation Flow>

Description will be given to examples of a partial isolation flow and a partial isolation and complete isolation combination flow.

[0190]

Figs. 38 to 52 are sectional views showing a partial isolation flow for forming an element in a first region isolated from a partial isolation region. The partial isolation flow will be described below with reference to these drawings.

[0191]

As shown in Fig. 38, first of all, an SOI substrate which is an initial wafer is prepared. The SOI substrate has a multilayered structure including a semiconductor substrate 1, the buried oxide film 2 and the SOI layer 4. Typically, the SOI layer 4 has a thickness of 30 to 400 nm and the buried oxide film 2 has a thickness of 100 to 500 nm. When used for power devices, the SOI layer 4 has a thickness of several to tens of

micrometers (μm).

[0192]

As shown in Fig. 39, next, an oxide film 35 is formed on a surface of the SOI layer 4. A thermal oxide film, a TEOS oxide film or the like is used as the oxide film 35. The oxide film 35 has a thickness of approximately 5 to 40 nm. Then, a nitride film 36 is deposited on the oxide film 35. The nitride film 36 has a thickness of 50 to 300 nm. The nitride film 36 may be deposited by LPCVD (Low Pressure Chemical Vapor deposition) or plasma nitride film CVD.

[0193]

Subsequently, the nitride film 36 is subjected to lithography. More specifically, by using a resist formed on the nitride film 36 as a mask, the nitride film 36 is patterned by an RIE (Reactive Ion Etching) or ECR (Electron Cyclotron Resonance) apparatus. Then, the resist is removed by ashing and SPM (Sulfuric acid-hydrogen Peroxide Mixture).

[0194]

As shown in Fig. 40, the oxide film 35 and the SOI layer 4 are etched by using the patterned nitride film 36 as a mask by means of the RIE or ECR apparatus. Thus, trenches 37 are selectively formed. In this case, the trenches 37 are formed so that part of the SOI layer 4 remains.

[0195]

As shown in Fig. 41, an oxide film 38 is deposited over the whole surface. The oxide film 38 may be deposited by using a plasma TEOS apparatus, an HDP (High Density Plasma) apparatus or the like. The oxide film 38 has a thickness of approximately 100 to 500 nm. Then, the surface is flattened by using a CMP (Chemical Mechanical Polishing) apparatus. As a result, the oxide film 38 is buried in the trenches

37.

[0196]

Thereafter, heat treatment is carried out at a temperature of 1000℃ to 1100℃ to improve the quality of the deposited oxide film 38. In the stage of Fig. 40 in which the oxide film 38 has not been deposited, it is effective to perform high temperature thermal oxidation at a temperature of 900℃ to 1000℃ on inner walls of the trenches 37 to round corner portions of the SOI layer 4 in upper and bottom parts of the trenches because stresses can be relieved.

[0197]

As shown in Fig. 42, the oxide film is etched back by RIE, ECR or wet etching. Then, the nitride film 36 is removed by using hot phosphoric acid. Thus, the partial oxide films 31 are completed. A region isolated by the partial oxide film 31 and the SOI layer 4 provided under the partial oxide film 31 serves as an element formation region. At this time, the oxide film 35 remaining on the SOI layer 4 (active) may be completely removed and a thermal oxide film or an oxide film may be deposited again.

[0198]

As shown in Fig. 43, B (boron) ions 40 are implanted to form the p well region 11 by using, as a mask, a resist 39 patterned by lithography.

[0199]

As shown in Fig. 44, P (phosphorus) ions 42 are implanted to form the n well region 12 by using, as a mask, a resist 41 patterned by lithography.

[0200]

In order to form the n well region 12, impurities such as As or Sb may be used in place of P. In order to form the p well region 11, BF2, In or the like may be used in place of B. Each of the p well region 11 and the n well region 12 is adjusted to have an

impurity concentration of 1×10^{15} to 1×10^{19} cm^{-2}.

[0201]

As shown in Fig. 45, the oxide film 35 formed on the surface of the SOI layer 4 is removed by wet etching, and an oxide film 56 for a gate oxide film is then formed. For the oxide film 56, it is also possible to use a metal oxide film such as Al_2O_3, a high dielectric oxide film such as Ta_2O_5 or BST, or the like as well as a thermal oxide film and an oxy-nitride film which are usually used.

[0202]

Next, a polysilicon layer is deposited to a thickness of approximately 100 to 400 nm by using the LPCVD device. A polysilicon layer doped with impurities such as P and B may be used as the polysilicon layer. Furthermore, a metal electrode such as W, Ta or Al may be used in place of the polysilicon layer as the material of the gate electrode.

[0203]

Next, lithography is carried out. Then, the polysilicon layer is processed by using an anisotropic etching apparatus such as RIE or ECR, to form the gate electrode 7. At this time, an insulation film such as an oxide film or a nitride/oxide film which is deposited on the polysilicon layer and subjected to lithography may be used as a mask to process the polysilicon layer. While the gate electrode 7 is typically shown in Fig. 45, gate electrodes such as the H gate electrode 71, the T gate electrode 72 or the special H gate electrode 73 may be formed, and a date electrode structure may be changed for each element formation region.

[0204]

As shown in Fig. 46, p-type impurities are implanted by using, as a mask, a resist 43 patterned by lithography and the gate electrode 7 to form pocket regions 11a.

The pocket regions 11a has the function of suppressing a short channel effect resulting from device size reduction. The short channel effect is also influenced by conditions such as the junction depth of the source/drain, the gate oxide film and the like. Therefore, if the conditions and the like are optimized to suppress the short channel effect, it is also possible to omit the step of forming the pocket regions.

[0205]

As the p-type impurities for the formation of the pocket regions, B, BF2 or In is implanted at approximately 1×10^{12} to 1×10^{14} cm^{-2} to form the pocket regions 11a.

[0206]

Furthermore, after the pocket regions are formed, n-type impurities are implanted by using the resist 43 and the gate electrode 7 as a mask to form n extension regions 44. As the n-type impurities, As, P or Sb may be used at approximately 1×10^{13} to 1×10^{15} cm^{-2}.

[0207]

As shown in Fig. 47, n-type impurities are implanted by using, as a mask, a resist 45 patterned by lithography and the gate electrode 7 to form pocket regions 12a.

[0208]

As the n-type impurities for the formation of the pocket regions, As, P or Sb is used at approximately 1×10^{12} to 1×10^{14} cm^{-2} to form the pocket regions 12a.

[0209]

Furthermore, after the formation of the pocket regions, p-type impurities are implanted by using the resist 45 and the gate electrode 7 as a mask to form n extension regions 46. As the p-type impurities, B, BF2 or In may be used at approximately 1×10^{13} to 1×10^{15} cm^{-2}.

[0210]

Although both the pocket regions 11a and the p extension regions 46 are shown as "p^-" for convenience in Figs. 46 and 47, the p extension regions 46 actually have a higher impurity concentration. Similarly, although both the pocket regions 12a and the n extension regions 44 are shown as "n^-" for convenience, the n extension regions 44 actually have a higher impurity concentration.

[0211]

In Figs. 48 and succeeding figures which will be described below, an NMOS transistor among the NMOS and PMOS transistors will be described as a representative. A PMOS transistor is formed in a manner similar to the NMOS transistor except that the conductivity type is opposite from that of the NMOS transistor.

[0212]

As shown in Fig. 48, side wall films are deposited on side surfaces of the gate electrode 7. A TEOS film or a plasma oxide film is used as the side wall films. Instead, an insulation film of Si_3N_4 formed by LPCVD or plasma CVD or an insulation film having a two-layer structure of Si_3N_4/SiO_2 may be used. After the deposition, etch back is carried out to form the side walls 6.

[0213]

Next, lithography is carried out, and n-type impurities are implanted into an NMOS formation region, to thereby form the source region 52 and the drain region 62. As the n-type impurities, As, P, Sb or the like is implanted at approximately 1×10^{14} to 1×10^{16} cm^{-2}. During the formation of the source region 52 and the drain region 62, an n-type body region of the PMOS may be formed together.

[0214]

Although not shown in Fig. 48, the source/drain regions of the PMOS may be formed by implanting p-type impurities such as B, BF2 or In at approximately 1×10^{14} to

1×10^{16} cm^{-2}. In this case, a p-type body region of the NMOS may be formed together. Subsequently, annealing (800 to 1150℃) for activating the source/drain regions is carried out.

[0215]

As shown in Fig. 49, the oxide film 56 on portions to be silicided (the source region 52, the drain region 62, the gate electrode 7, a body region (not shown) or the like) is removed. Thus, only the oxide film 56 under the gate electrode 7 and the side walls 6a remains. The oxide film 56 under the gate electrode 7 becomes the gate oxide film 5, and the oxide film 56 under the side walls 6a and the side walls 6a become the side walls 6. Then, silicide regions 47, 48 and 49 are formed on the surfaces of the source region 52, the drain region 62 and the gate electrode 7.

[0216]

In this case, formation of at least two of the PDSOI-MOSFETs of types 1 to 7 in at least two element formation regions isolated by the partial isolation region provides the semiconductor device according to the fifth embodiment.

[0217]

Fig. 49 shows a salicide process which performs silicidation also on the source, the drain and the gate. A polycide process which silicides only the gate and some applications (ESD: Electro-Static Discharge and the like) form a silicide protection oxide film on the source, the drain and the gate, and do not perform complete silicidation. The silicide used herein includes $TiSi_2$, $CoSi_2$, $NiSi_2$, WSi_2, $TaSi_2$, $MoSi_2$, $HfSi_2$, Pd_2Si, PtSi, $ZrSi_2$ and the like.

[0218]

As shown in Fig. 50, an interlayer insulation film 85 which is an oxide film is deposited in a thickness of approximately 1 μm over the whole surface. Then, CMP is

carried out to flatten the interlayer insulation film 85. Thereafter, lithography for contact formation is carried out, and contact holes 84 are formed on the silicide regions 47 and 48 by etching.

[0219]

As shown in Fig. 51, W (tungsten) is deposited over the whole surface. Al, TiN, or a D-polysilicon layer may be deposited in place of W. For W, a film deposition method includes a blanket CVD process and a selective CVD process. For Al, a high-temperature sputtering process and a reflow sputtering process may be used. For TiN and the D-polysilicon layer, an LPCVD process may be used. In order to enhance adhesion of W and the underlying insulation film, Ti, TiN and TiW may be formed before W is deposited. Description will be given on W in the blanket CVD process. After W is deposited, it is completely flattened by etch back.

[0220]

As shown in Fig. 52, an aluminum wiring layer 88 serving as a first-layer metal is deposited. As a matter of course, AlCuSi, Cu or a D-polysilicon layer may be used as the material of the aluminum wiring layer 88. After lithography, the aluminum wiring layer 88 is processed.

[0221]

Then, an interlayer insulation film 87 is deposited over the whole surface including the aluminum wiring layer 88, and is flattened by using a CMP technique or the like to eliminate surface irregularities.

[0222]

As shown in Fig. 53, a hole (via hole) for connection to a metal interconnect line serving as a second-layer metal is opened and filled with a tungsten layer 89 in a manner similar to the contact. Then, an aluminum wiring layer 97 serving as the

second-layer metal is formed in a manner similar to the first-layer metal. Thereafter, an interlayer insulation film 96 is provided over the whole surface and is flattened in a manner similar to the interlayer insulation film 87.

[0223]

Subsequently, in the case of a device requiring a metal interconnect line serving as at least a third-layer metal, the method further comprises repeating the step shown in Fig. 52 or 53, depositing a chip protective film (passivation film), and opening a window (pad) for bonding wire connection. Thus, all steps are completed.

[0224]

While the Dual gate process using the n^+ gate and the p^+ gate has been described as the CMOS step, it is a matter of course that a Single gate process or a metal gate (W, Ta or the like) process may be used.

[0225]

<Partial Isolation and Complete Isolation Combination Flow>

Figs. 54 to 57 are sectional views showing the steps of forming the complete isolation region in a method of manufacturing a semiconductor device for the partial isolation and complete isolation combination. With reference to these drawings, a partial isolation and complete isolation combination flow will be described.

[0226]

First of all, the partial isolation flow shown in Figs. 38 to 40 is executed. As shown in Fig. 54, the trench 37 is additionally etched by using, as a mask, a resist 98 patterned by lithography, and a portion to be completely isolated is etched through the SOI layer 4. Thus, a trench 57 reaching the buried oxide film 2 is formed.

[0227]

As shown in Fig. 55, the resist 98 is removed and an oxide film 99 is then

deposited over the whole surface. The oxide film 99 is deposited by using a plasma TEOS or HDP apparatus or the like. The oxide film 99 has a thickness of approximately 100 to 500 nm. A difference t1 in depth between the trench 37 for partial isolation and the trench 57 for complete isolation causes a level difference t2 reflecting the difference t1 shown between the level of the oxide film 99 over the trench 37 and the level thereof over the trench 57.

[0228]

As shown in Fig. 56, a surface is flattened by using a CMP apparatus so that the oxide film 99 is buried in the trench 37 and an oxide film 100 is buried in the trench 57. However, the above-mentioned level difference t2 between the oxide film 99 in the partial isolation region and the oxide film 99 in the complete isolation region causes dishing in the complete isolation portion (oxide film 100). Thereafter, heat treatment is carried out at a temperature of 1000℃ to 1100℃ to improve the quality of the deposited film. Before the oxide film deposition, it is effective to perform high-temperature thermal oxidation at a temperature of 900℃ to 1000℃ on the inner surfaces of the trench to round corner portions of the SOI layer 4 in upper and bottom parts of the trench because stresses can be relieved.

[0229]

As shown in Fig. 57, the oxide films 99 and 100 are etched back by RIE, ECR or wet etching. Then, the oxide film 35 is removed by using hot phosphoric acid. As a result, the partial oxide film 31 and the complete oxide film 32 are completed. This produces the first element formation region isolated from its surroundings by the partial oxide film 31, and the second element formation region isolated from its surroundings by the complete oxide film 32. At this time, the oxide film 35 remaining on the surface (active) of the SOI layer 4 may be removed completely and a thermal oxide film or an

oxide film may be deposited again.

[0230]

Fig. 58 is a sectional view showing the partial isolation region and its surroundings when the polysilicon layer 70 for the gate electrode 7 is formed. As shown in Fig. 58, when the polysilicon layer 70 is formed to have a thickness t0, part of the polysilicon layer 70 near the edge of the partial oxide film 31 has a thickness t11 (> t0) reflecting a comparatively great level difference between the partial oxide film 31 and the oxide film 56.

[0231]

Fig. 59 is a sectional view showing the complete isolation region and its surroundings when the polysilicon layer 70 for the gate electrode 7 is formed. As shown in Fig. 59, when the polysilicon layer 70 is formed to have the thickness t0, part of the polysilicon layer 70 near the edge of the complete oxide film 32 has a thickness t12 (> t0) reflecting a comparatively small level difference between the complete oxide film 32 and the oxide film 56.

[0232]

In this manner, the partial oxide film 31 for partial isolation and the complete oxide film 32 for complete isolation have different isolation edge shapes which are edge shapes thereof. This results in the fact that the level difference between the partial oxide film 31 and the oxide film 56 is greater than the level difference between the complete oxide film 32 and the oxide film 56. Consequently, t11 > t12 is established.

[0233]

During the etching process on the polysilicon layer 70 for achievement of the gate electrode 7 shown in Fig. 45, an etching parameter such as etch time is determined so that part of the polysilicon layer 70 having the maximum thickness t11 is removed

reliably.

[0234]

For this reason, the portion having the thickness t12 is overetched by the amount (t11 – t12) to suffer increased etching damages (plasma damages). As a result, there is apprehension that the reliability of the oxide film 56 serving as the gate oxide film near the edge of the complete oxide film 32 might be deteriorated.

[0235]

In this respect, the H gate electrode has the "I" portions which cover more isolation edge portions than a normal gate to suppress the deterioration of the reliability of the gate oxide film in the isolation edge portion.

[0236]

More specifically, the isolation edge portion susceptible to damages becomes effectively smaller by the formation of the H gate electrode. In a transistor fabricated in the complete isolation portion having the low isolation edge shape, there is apprehension that leakage current is increased by a local parasitic MOS which comes from a drop in threshold voltage due to the reduction in gate oxide film thickness. This problem can also be solved by the H gate electrode according to the present invention.

[0237]

In the subsequent steps, for example, any one of the PDSOI-MOSFETs of the types 1 to 7 is formed on the first element formation region isolated by the partial isolation region in the same manner as in the steps shown in Figs. 42 to 54 of the partial isolation flow, and any one of the PDSOI-MOSFETs of the types A to F is formed on a second element isolation region isolated by the complete isolation region. Thus, the semiconductor device according to the sixth embodiment is completed.

[0238]

[Effects of the Invention]

As described above, in the semiconductor device according to claim 1 of the present invention, the body region potential setting portion whose potential is externally fixable is provided in the element formation region. Therefore, it is possible to fix a body potential which is the electric potential of the body region main part with high stability.

[0239]

In the semiconductor device according to claim 2, the gate extension region of the gate electrode electrically cuts off the body region source/drain adjacent portion and the source and drain regions. The presence of the body region source/drain adjacent portion does not affect the operation of the MOS transistor, and the body potential can be fixed with high stability.

[0240]

In the semiconductor device according to claim 3, the body potential can be fixed from the first and second body region source/drain adjacent portions. It is possible to accordingly fix the body potential with higher stability.

[0241]

In the semiconductor device according to claim 4, the one body region source/drain adjacent portion can fix the body potential with high stability while the one gate extension region minimizes the gate capacitance.

[0242]

In the semiconductor device according to claim 5, the body region source/drain adjacent portion has the high concentration region having the higher impurity concentration than that of other regions and spaced the predetermined distance apart from the gate extension region. Therefore, during the implantation of impurities of the second

conductivity type for the formation of the high concentration region, the impurities of the second conductivity type are reliably prevented from being implanted into the gate extension region.

[0243]

In the semiconductor device according to claim 6, the gate extension region of the second conductivity type has the impurity concentration of not greater than 5×10^{18} cm^{-2}. This suppresses variations in threshold voltage of the MOS transistor.

[0244]

In the semiconductor device according to claim 7, fixation of the electric potential of the body potential fixing semiconductor region of the second conductivity type which is formed together with the source region allows the fixation of the body potential with high stability. The presence of the body potential fixing semiconductor region does not affect the MOS transistor which operates with the body region and the source region set at the same potential.

[0245]

In the semiconductor device according to claim 8, it is possible to fix the electric potential of the body region from the outside-element-formation-region body region through the under-partial-insulation-film semiconductor region, in addition to the body region potential setting portion.

[0246]

In the semiconductor device according to claim 9, the source and drain regions of the MOS transistor have such depths as to reach the buried insulation layer. Therefore, no pn junction is formed on the bottom faces thereof. This suppresses junction leakage.

[0247]

In the semiconductor device according to claim 10, the source and drain regions of the MOS transistor have such depths that the depletion layer extending from the source and drain regions does not reach the buried insulation layer during the normal operation. Therefore, in the case in which the electric potential of the body region is to be fixed from outside the element formation region, the body potential fixation can be carried out with high stability.

[0248]

In the semiconductor device according to claim 11, the source and drain regions of the MOS transistor do not reach the buried insulation layer, and the depletion layer extending from the drain region has such a depth as to reach the buried insulation layer during the normal operation. Therefore, it is possible to fix the body potential from outside the element formation region while reducing a junction capacitance.

[0249]

In the semiconductor device according to claim 12, the depth is greater than that of the source region of the MOS transistor, and the depth is such that the depletion layer extending from the drain region reaches the buried insulation layer during the normal operation. Therefore, it is possible to reduce the junction capacitance in the drain region while fixing the body potential through under the source region from outside the element formation region.

[0250]

In the semiconductor device according to claim 13, the under-partial-insulation-film semiconductor region of the predetermined conductivity type which is part of the SOI layer provided under the partial insulation film is used as a component of the resistive element. Therefore, it is possible to obtain the resistive element having a high resistance value with a comparatively small formation area. As a

result, it is possible to constitute a semiconductor integrated circuit having a high degree of integration.

[0251]

In the semiconductor device according to claim 14, the complete insulation film can completely isolate the resistive element from the outside.

[0252]

In the semiconductor device according to claim 15, the element formation region except in the partial insulation film and the first and second semiconductor regions is used as a part of the region where the resistive element is to be formed. This suppresses variations in resistance value of the resistive element.

[0253]

The semiconductor device according to claim 16 uses the resistive element as the load resistor of an SRAM, to constitute the SRAM having a high degree of integration.

[0254]

In the semiconductor device according to claim 17 of the present invention, the first and second MOS transistors are made different from each other in at least one of a body region structure, a gate electrode structure and the presence/absence of body potential fixation, thereby to have different transistor characteristics. This provides a high functional semiconductor integrated circuit comprising the first and second MOS transistors.

[0255]

In the semiconductor device according to claim 18 of the present invention, the difference is made in transistor characteristic between the first MOS transistor isolated by the partial isolation region and the second transistor isolated by the complete isolation

region. This provides a high functional semiconductor integrated circuit comprising the first and second MOS transistors.

[0256]

In the semiconductor device manufactured by the method of manufacturing the semiconductor device according to claim 19 of the present invention, the first and second MOS transistors are made different from each other in at least one of a body region structure, a gate electrode structure and the presence/absence of body potential fixation, thereby to have different transistor characteristics. This provides a high functional semiconductor integrated circuit comprising the first and second MOS transistors.

[0257]

In the semiconductor device manufactured by the method of manufacturing the semiconductor device according to claim 20 of the present invention, the difference is made in transistor characteristic between the first MOS transistor isolated by the partial isolation region and the second transistor isolated by the complete isolation region. This provides a high functional semiconductor integrated circuit comprising the first and second MOS transistors.

[Brief Description of the Drawings]

[Fig. 1] is a sectional view showing an example of a conventional PDSOI-MOSFET.

[Fig. 2] is a plan view showing the example of the conventional PDSOI-MOSFET.

[Fig. 3] is a plan view showing a planar structure of a semiconductor device according to a first embodiment (first mode) of the present invention.

[Fig. 4] is a sectional view showing a section taken along the line A2-A2 of Fig. 3.

[Fig. 5] is a sectional view showing a section taken along the line B1-B1 of Fig. 3.

[Fig. 6] is a sectional view showing a second mode of the first embodiment.

[Fig. 7] is a sectional view showing a third mode of the first embodiment.

[Fig. 8] is a sectional view showing a fourth mode of the first embodiment.

[Fig. 9] is a plan view showing a planar structure of a semiconductor device according to a second embodiment of the present invention.

[Fig. 10] is a plan view showing a planar structure of a semiconductor device according to a third embodiment of the present invention.

[Fig. 11] is a sectional view showing a section taken along the line A4-A4 of Fig. 10.

[Fig. 12] is a sectional view showing a section taken along the line A5-A5 of Fig. 11.

[Fig. 13] is a plan view showing a planar structure of a semiconductor device according to a first mode of a fourth embodiment of the present invention.

[Fig. 14] is a plan view showing a planar structure of a semiconductor device according to a twelfth mode of the fourth embodiment of the present invention.

[Fig. 15] is a plan view showing a planar structure of a semiconductor device according to a third mode of the fourth embodiment of the present invention.

[Fig. 16] is a plan view showing a planar structure of a type 5 (No. 1) of a PDSOI-MOSFET.

[Fig. 17] is a plan view showing a planar structure of the type 5 (No. 2) of the PDSOI-MOSFET.

[Fig. 18] is a sectional view showing a sectional structure of a PDSOI-MOSFET of a type A.

[Fig. 19] is a plan view showing a planar structure of the PDSOI-MOSFET of the type A.

[Fig. 20] is a plan view showing a planar structure of a PDSOI-MOSFET of a type B.

[Fig. 21] is a plan view showing a planar structure of a PDSOI-MOSFET of a type D.

[Fig. 22] is a view conceptually showing a planar structure of a semiconductor device according to a sixth embodiment.

[Fig. 23] is a circuit diagram showing a first application of the semiconductor device according to the sixth embodiment.

[Fig. 24] is a circuit diagram showing a twenty-first application of the semiconductor device according to the sixth embodiment.

[Fig. 25] is a sectional view showing a structure of a completely isolated FDSOI-MOSFET.

[Fig. 26] is a sectional view showing a resistive element formation region of a semiconductor device according to a first mode of a seventh embodiment of the present invention.

[Fig. 27] is a plan view showing the first mode of the seventh embodiment.

[Fig. 28] is a sectional view showing a general resistive element formation region.

[Fig. 29] is a sectional view showing a resistive element formation region of a semiconductor device according to a second mode of the seventh embodiment.

[Fig. 30] is a sectional view showing a resistive element formation region of a semiconductor device according to a third mode of the seventh embodiment.

[Fig. 31] is a circuit diagram showing an SRAM cell having a 6-transistor

CMOS structure.

[Fig. 32] is a plan view showing a layout structure for implementing the SRAM cell illustrated in Fig. 31.

[Fig. 33] is a circuit diagram showing an SRAM cell having a high resistance load type cell structure.

[Fig. 34] is a plan view showing a layout structure for implementing the SRAM cell illustrated in Fig. 33.

[Fig. 35] is a plan view showing a general H gate electrode.

[Fig. 36] is a plan view showing a planar structure of a semiconductor device according to an eighth embodiment of the present invention.

[Fig. 37] is a sectional view showing a section taken along the line D1-D1 of Fig. 36.

[Fig. 38] is a sectional view showing a partial isolation flow.

[Fig. 39] is a sectional view showing the partial isolation flow.

[Fig. 40] is a sectional view showing the partial isolation flow.

[Fig. 41] is a sectional view showing the partial isolation flow.

[Fig. 42] is a sectional view showing the partial isolation flow.

[Fig. 43] is a sectional view showing the partial isolation flow.

[Fig. 44] is a sectional view showing the partial isolation flow.

[Fig. 45] is a sectional view showing the partial isolation flow.

[Fig. 46] is a sectional view showing the partial isolation flow.

[Fig. 47] is a sectional view showing the partial isolation flow.

[Fig. 48] is a sectional view showing the partial isolation flow.

[Fig. 49] is a sectional view showing the partial isolation flow.

[Fig. 50] is a sectional view showing the partial isolation flow.

[Fig. 51] is a sectional view showing the partial isolation flow.

[Fig. 52] is a sectional view showing the partial isolation flow.

[Fig. 53] is a sectional views showing a complete isolation flow.

[Fig. 54] is a sectional views showing the complete isolation flow.

[Fig. 55] is a sectional views showing the isolation flow.

[Fig. 56] is a sectional views showing the isolation flow.

[Fig. 57] is a sectional views showing the isolation flow.

[Fig. 58] is a sectional view showing a partial isolation region and its surroundings when a polysilicon layer for a gate electrode is formed.

[Fig. 59] is a sectional view showing a complete isolation region and its surroundings when the polysilicon layer for the gate electrode is formed.

[Reference Numerals and Characters]

2 buried oxide film; 4 SOI layer; 5 gate oxide film; 6 side wall; 7 gate electrode; 10, 13 body regions; 11 p well region; 17a p^+ body region; 17b p^- body region; 21, 22, 55 p^+ regions; 31 partial oxide film; 51-54 source regions; 61-63 drain regions; 71 H gate electrode; 72 T gate electrode; 73 special H gate electrode; 131A-131G partial isolation regions; 132 complete isolation region; R3, R34 resistive elements.

[Document Name] Abstract

[Abstract]

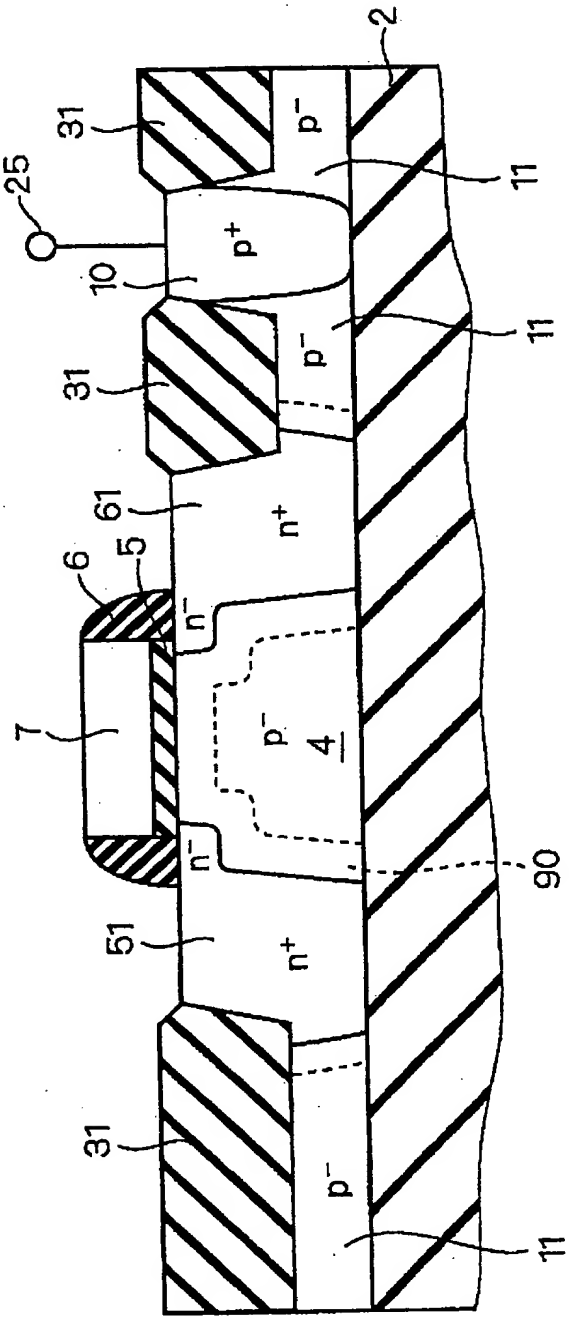
[Object] To provide a semiconductor device having an SOI structure capable of stably fixing the electric potential of a body region in an element formation region isolated by a partial isolation region.

[Means for Solution] A MOS transistor comprising a source region 51, a drain region 61 and an H gate electrode 71 is formed in an element formation region isolated by a partial oxide film 31. The H gate electrode 71 has left and right (in the figure, upper and lower) "I"s for electrically isolating body regions 13 formed adjacent in a gate width W direction to the source region 51 and the drain region 61 from the drain region 61 and the source region 51, and a central "–" functioning as a gate electrode of an original MOS transistor.

[Selected Figure] Fig. 3

[DOCUMENT NAME] DRAWINGS

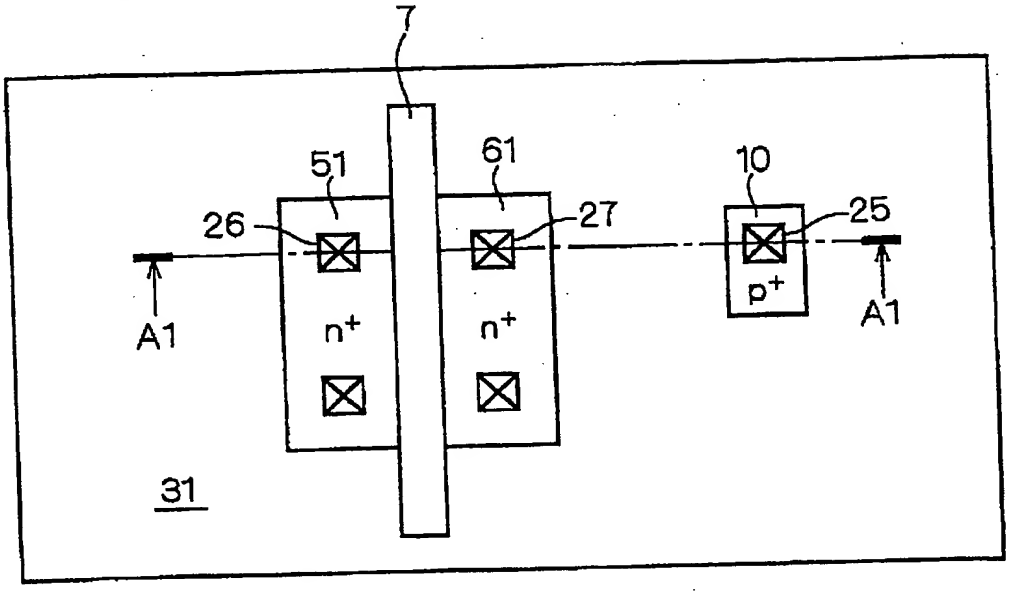
[FIG. 1]



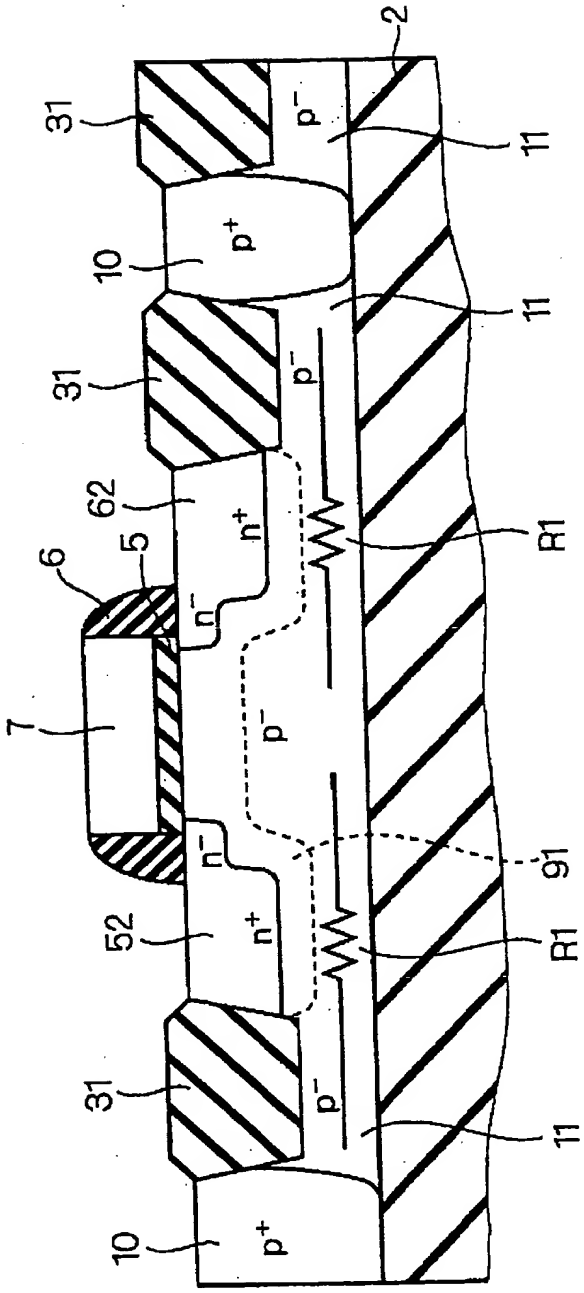
10: BODY REGION
11: p WELL REGION
31: PARTIAL OXIDE FILM
51: SOURCE REGION
61: DRAIN REGION

2: BURIED OXIDE FILM
4: SOI LAYER
5: GATE OXIDE FILM
6: SIDE WALL
7: GATE ELECTRODE

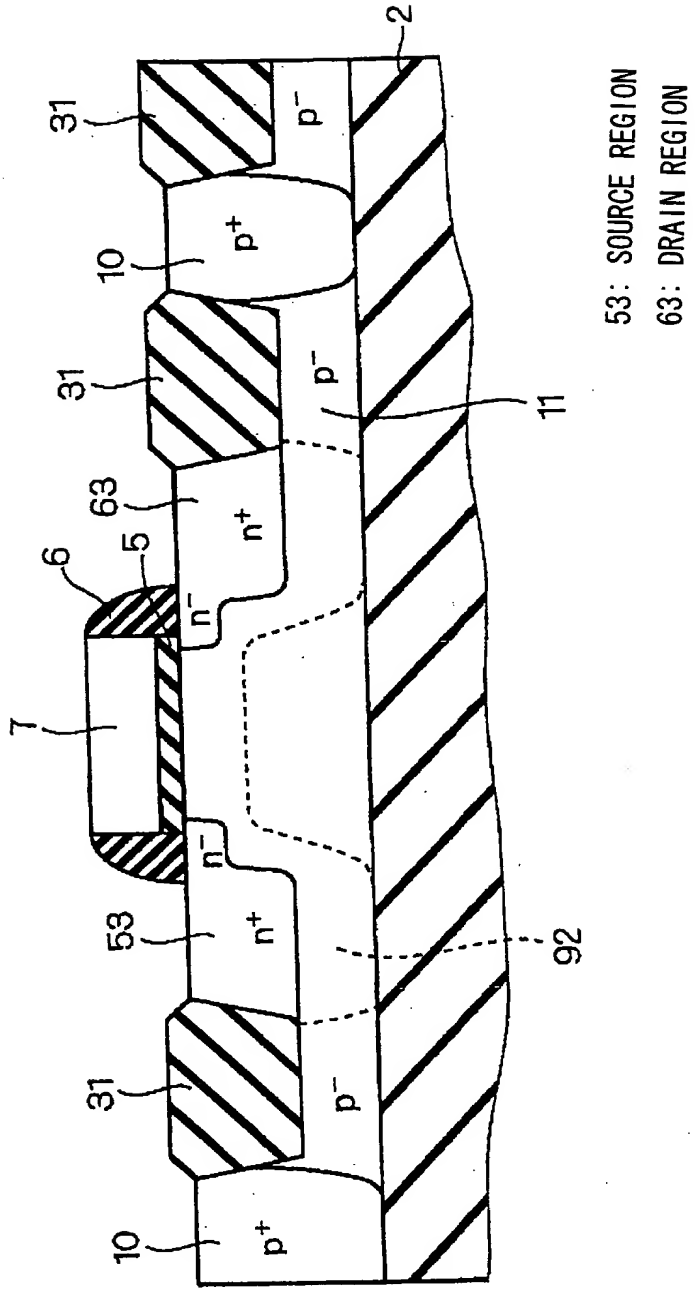
[FIG. 2]



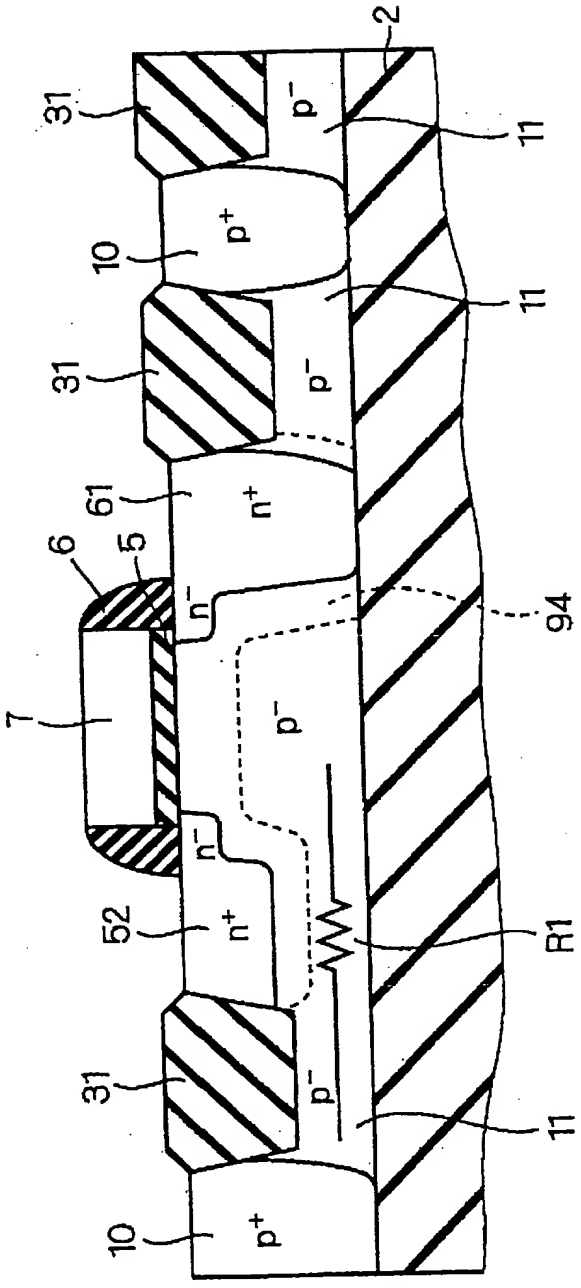
[FIG. 6]



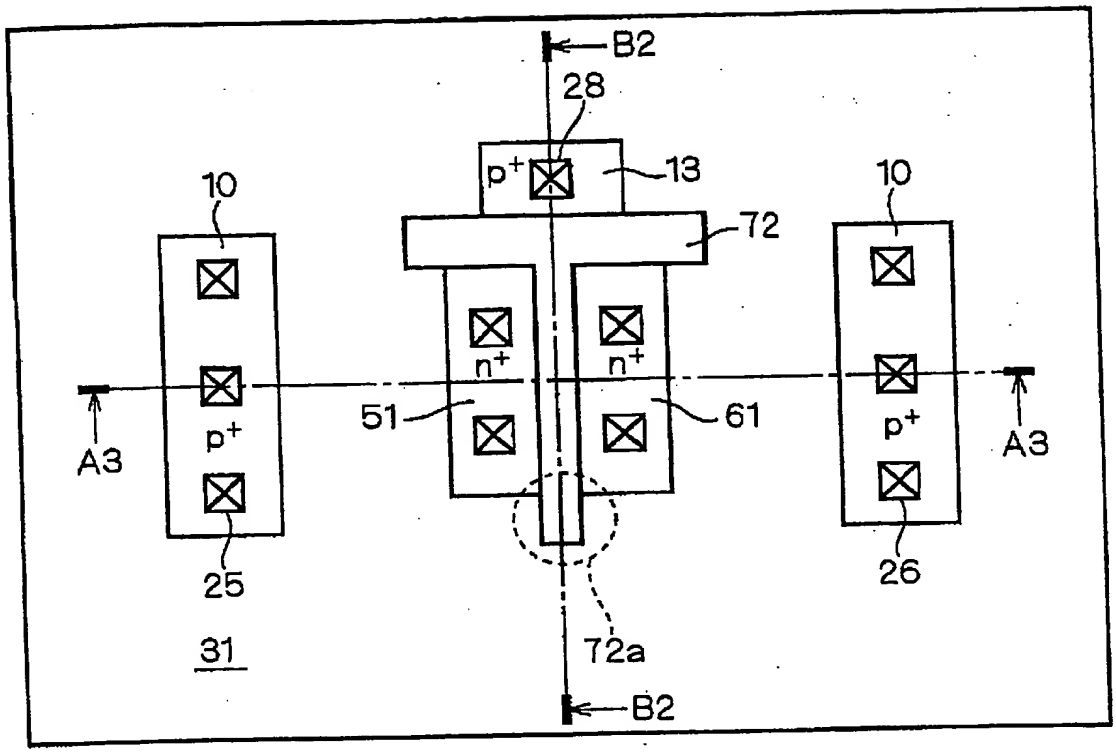
[FIG. 7]



[FIG. 8]

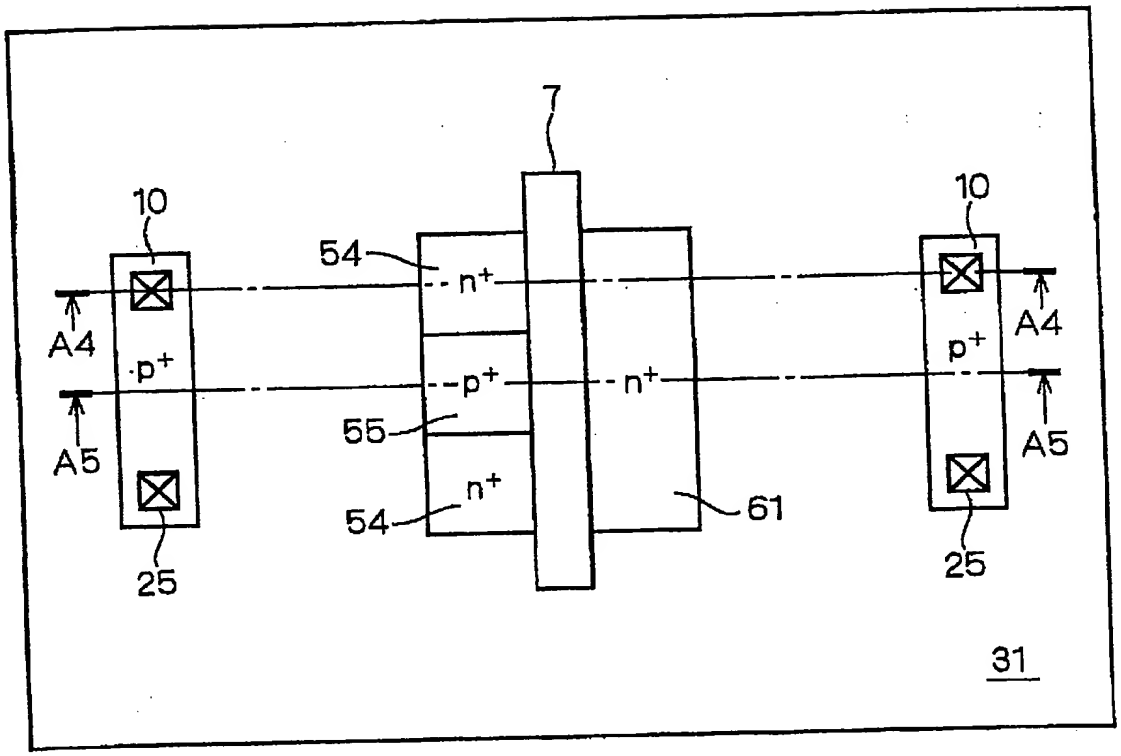


[FIG. 9]



72: T GATE ELECTRODE

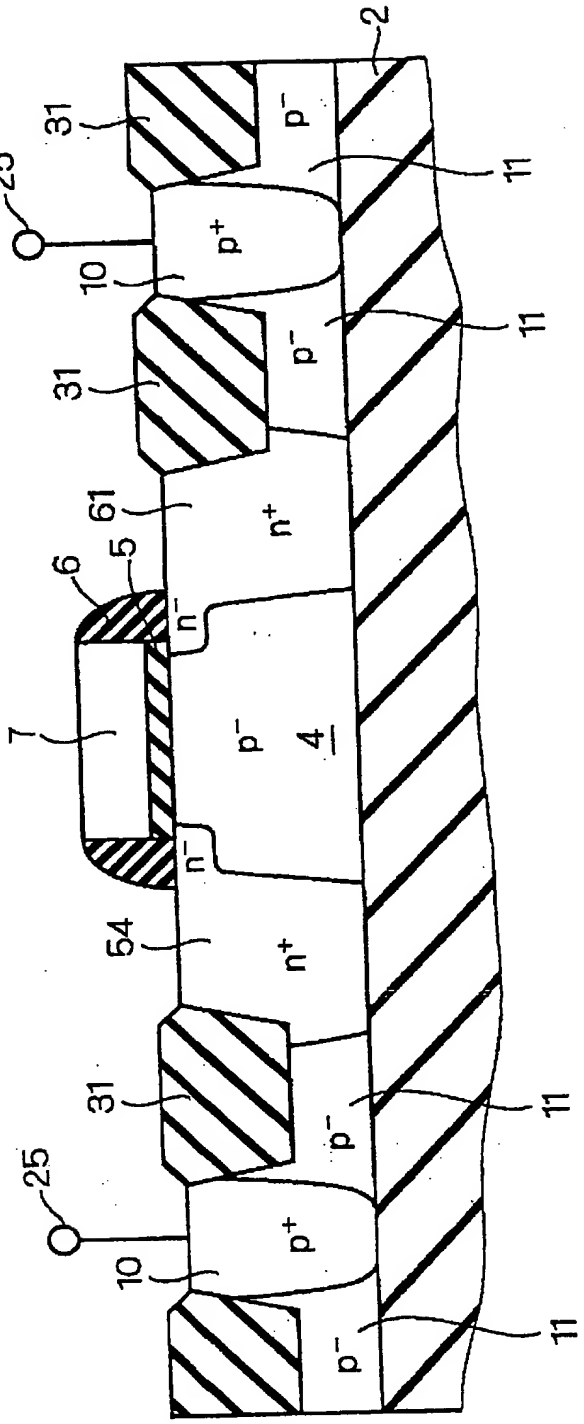
[FIG. 10]



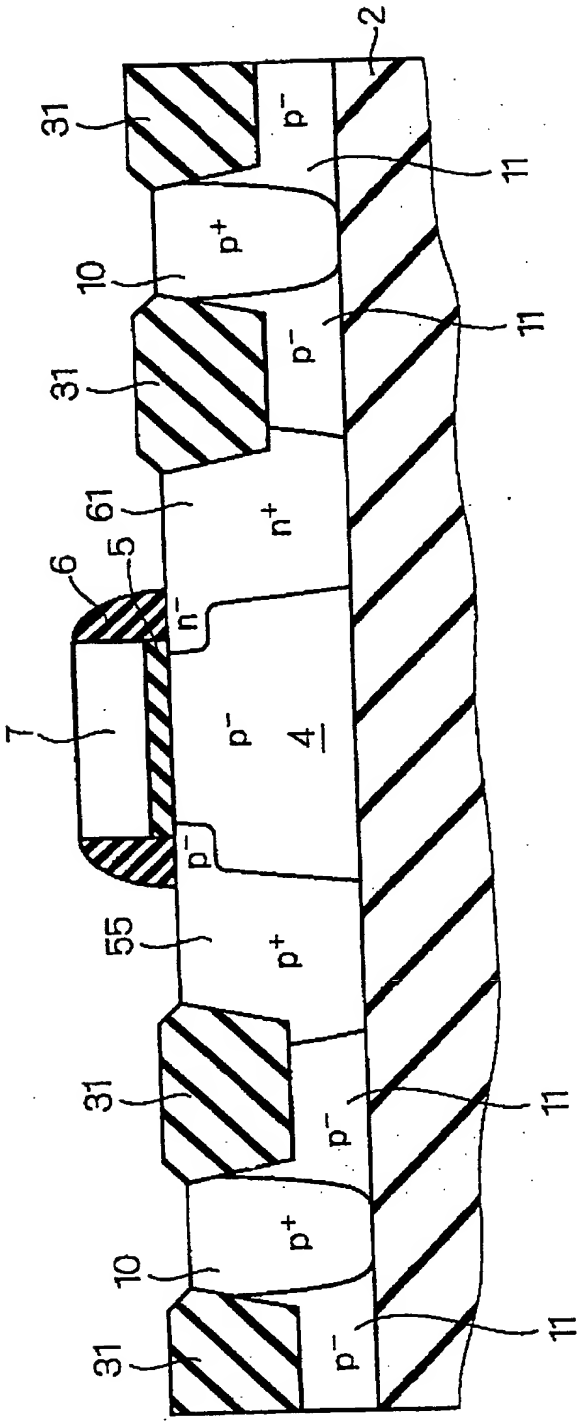
54: SOURCE REGION

55: p^+ REGION

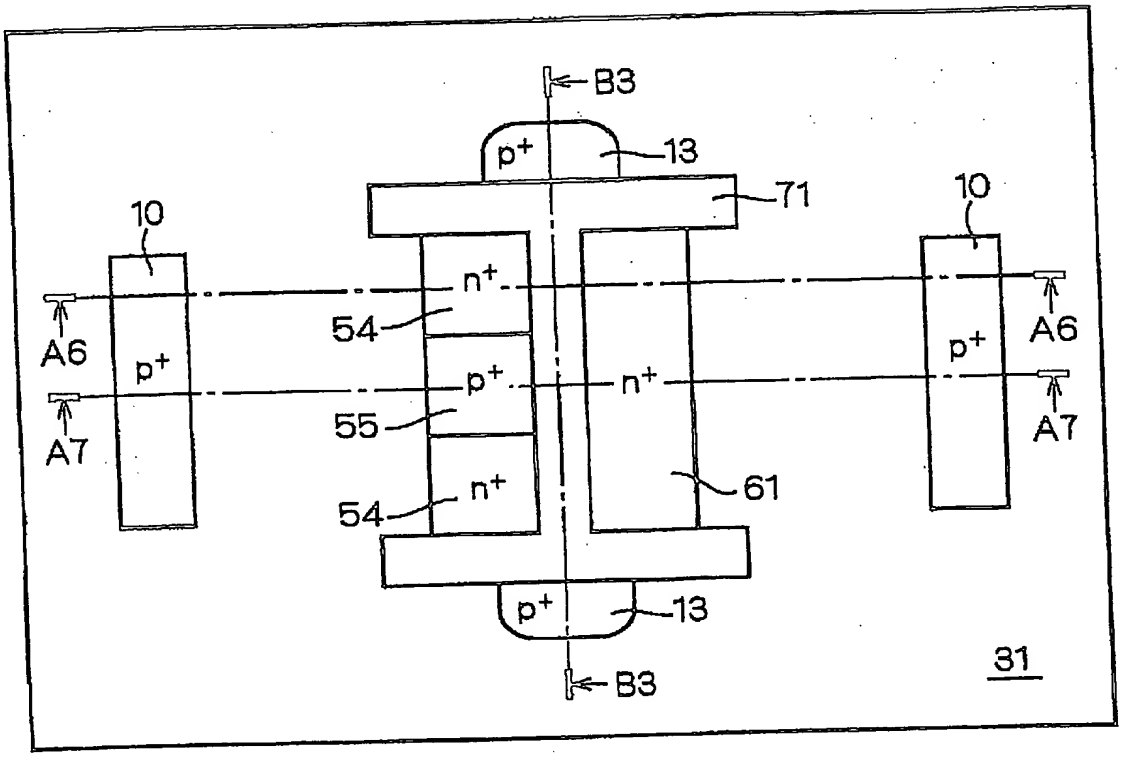
[FIG. 11]



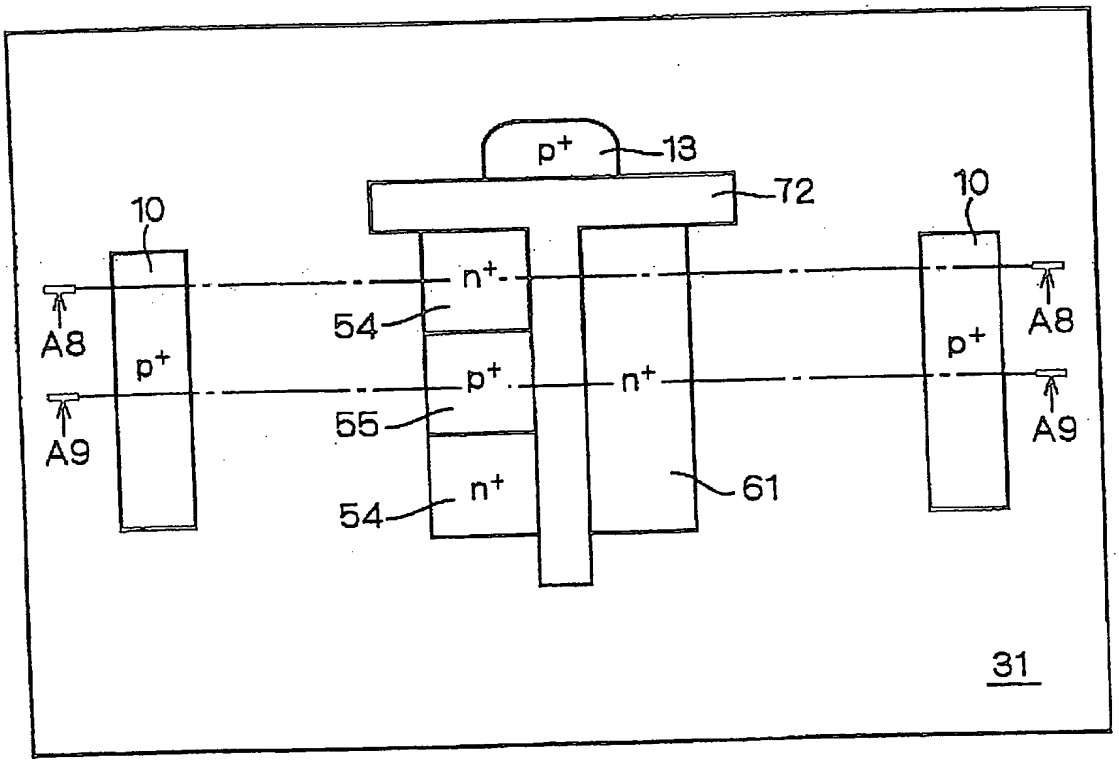
[FIG. 12]



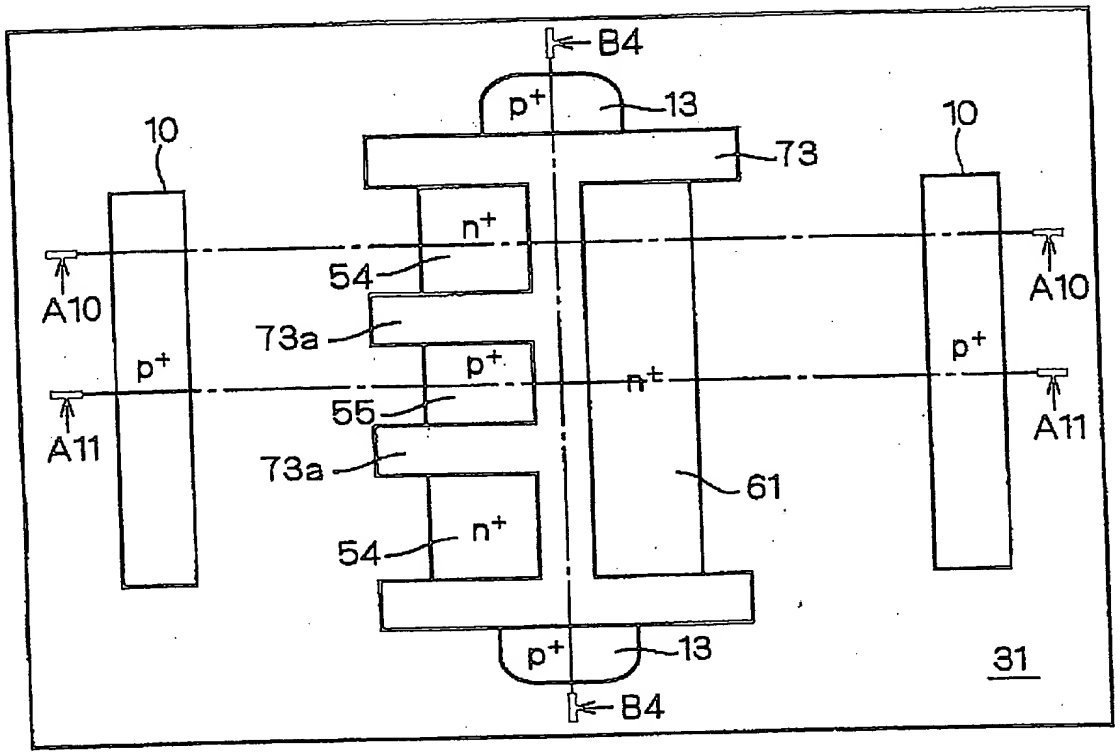
[FIG. 13]



[FIG. 14]

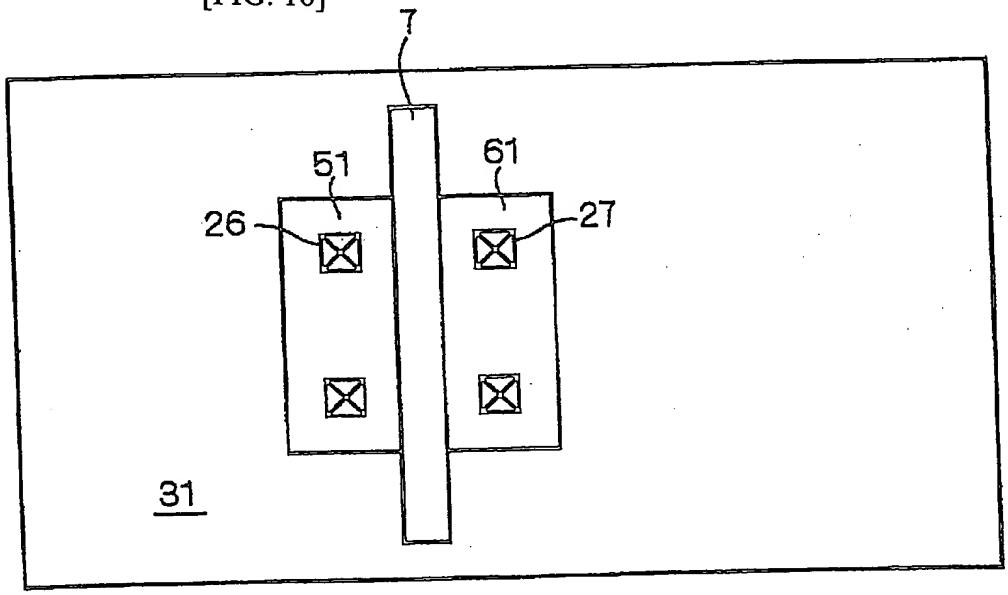


[FIG. 15]

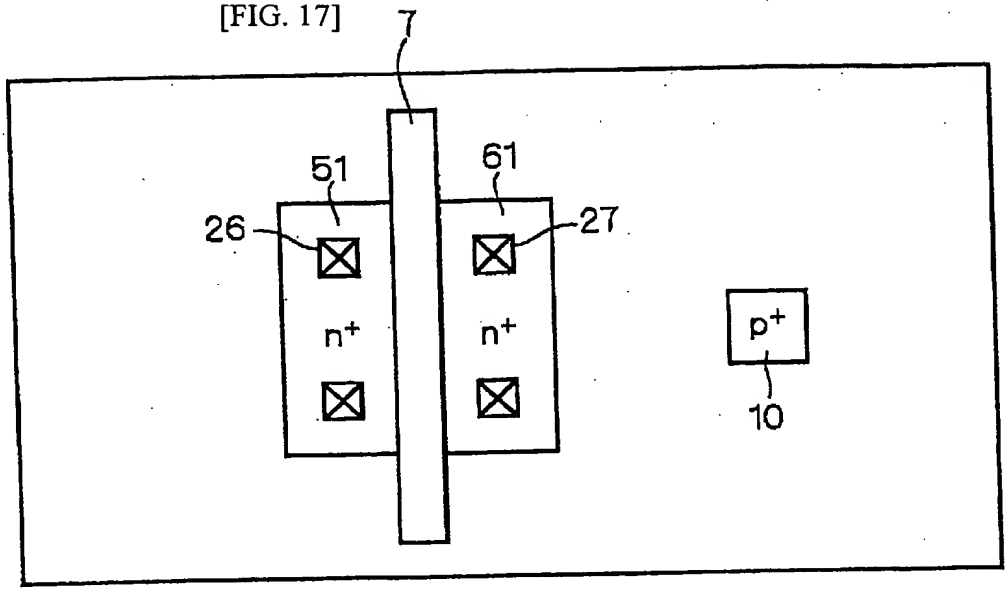


73: SPECIAL H GATE ELECTRODE

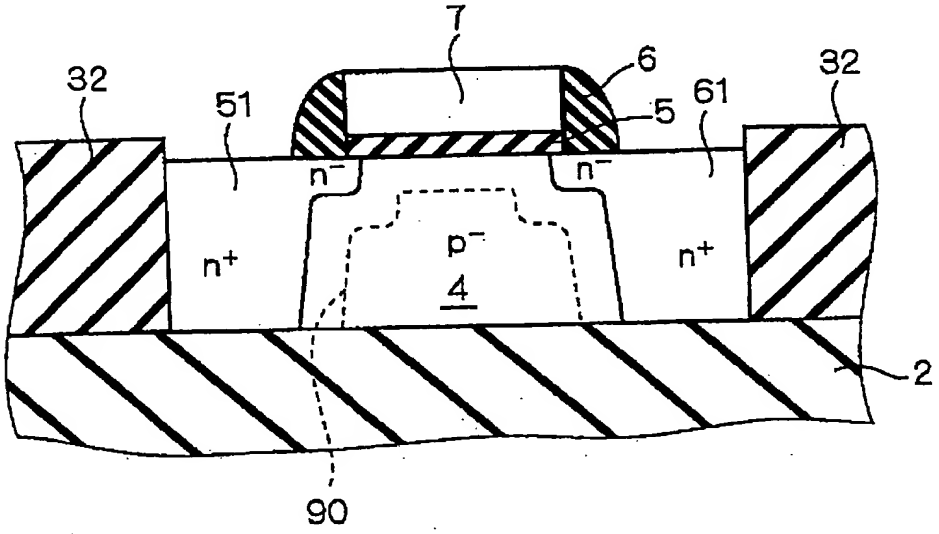
[FIG. 16]



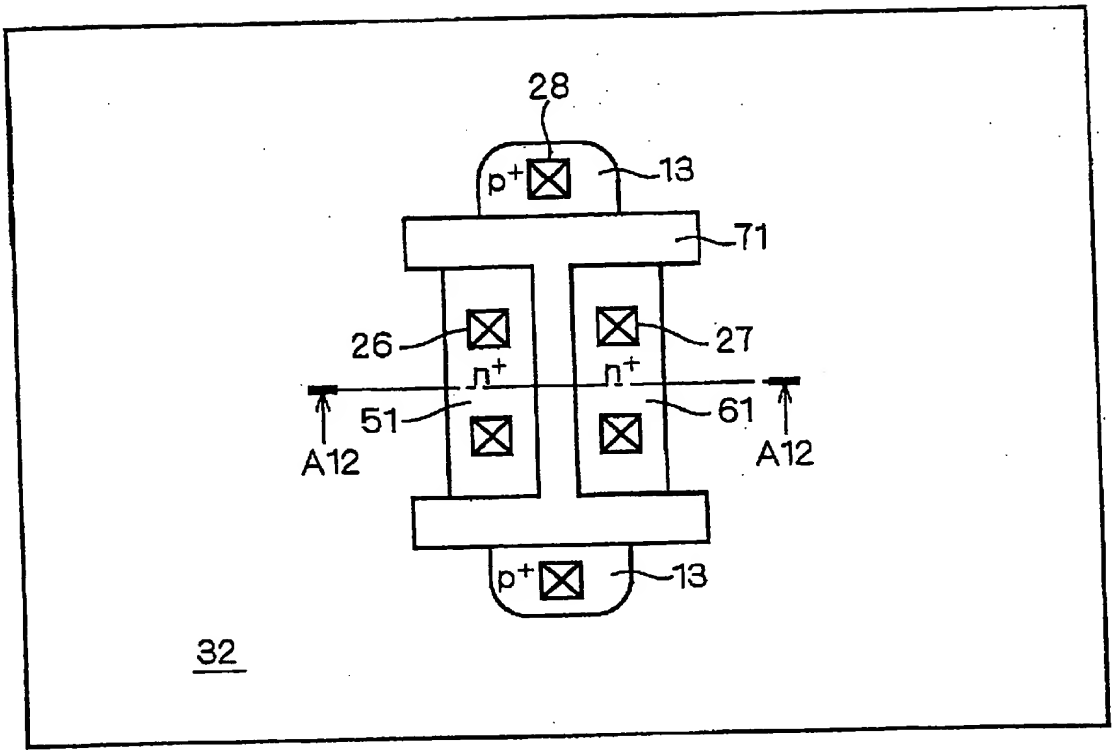
[FIG. 17]



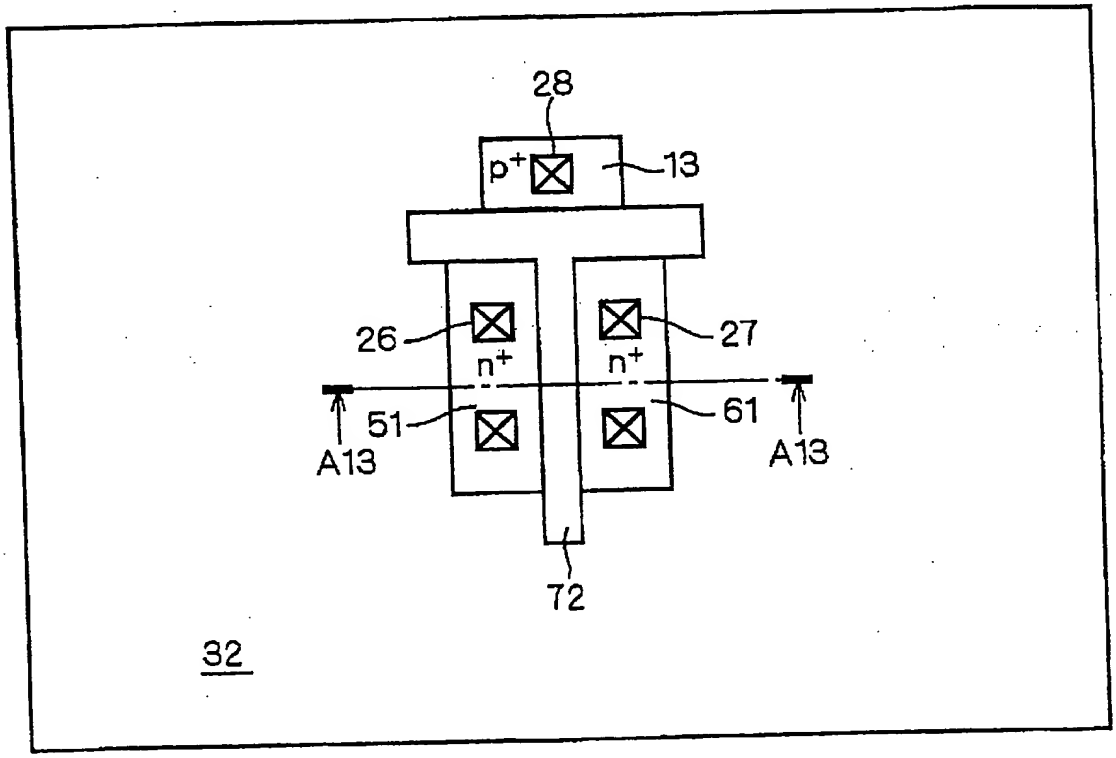
[FIG. 18]



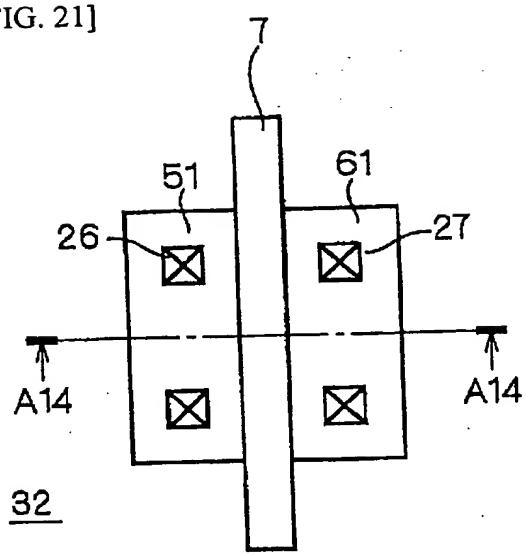
[FIG. 19]



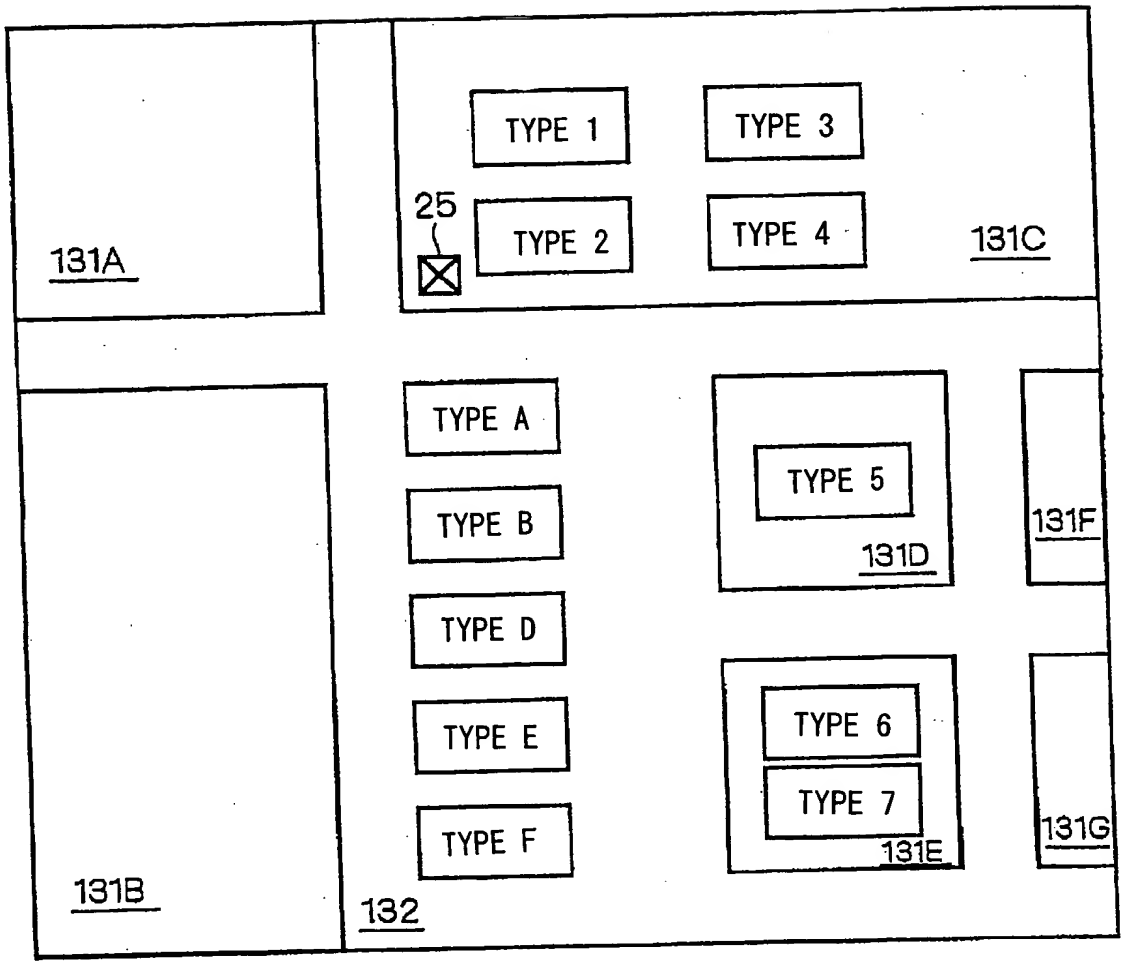
[FIG. 20]



[FIG. 21]

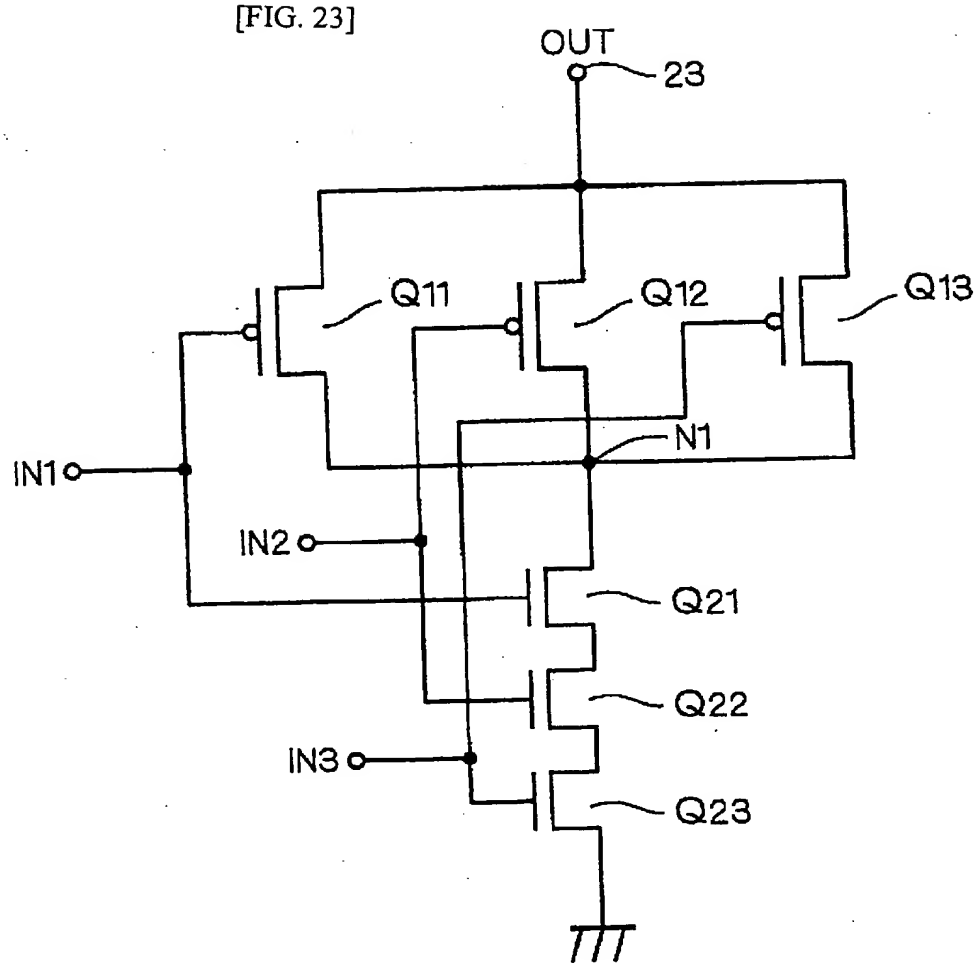


[FIG. 22]

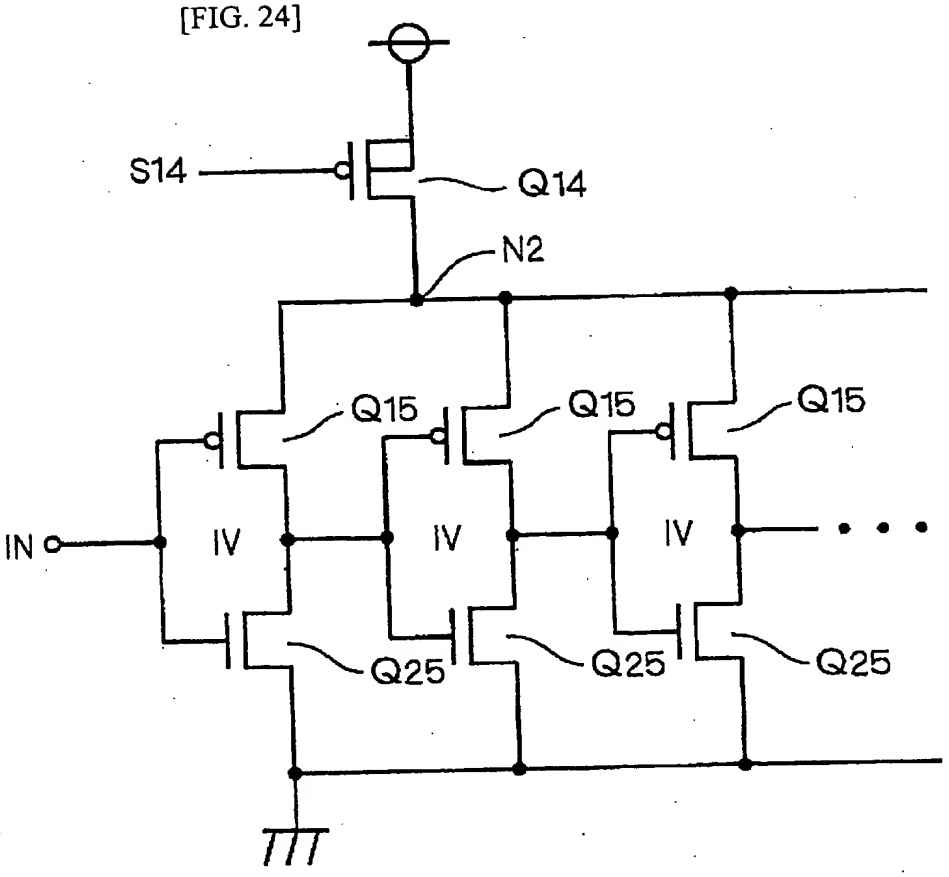


131A-131G: PARTIAL ISOLATION REGIONS
132: COMPLETE ISOLATION REGION

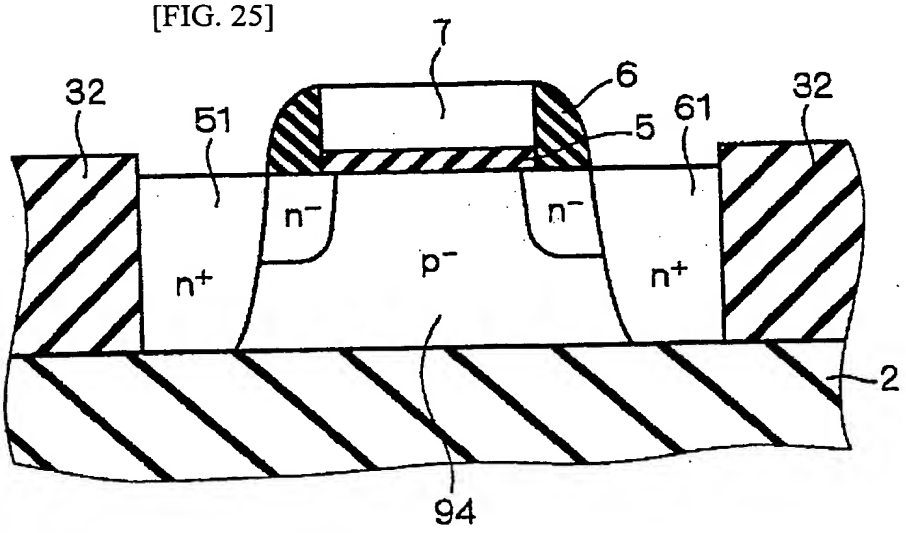
[FIG. 23]



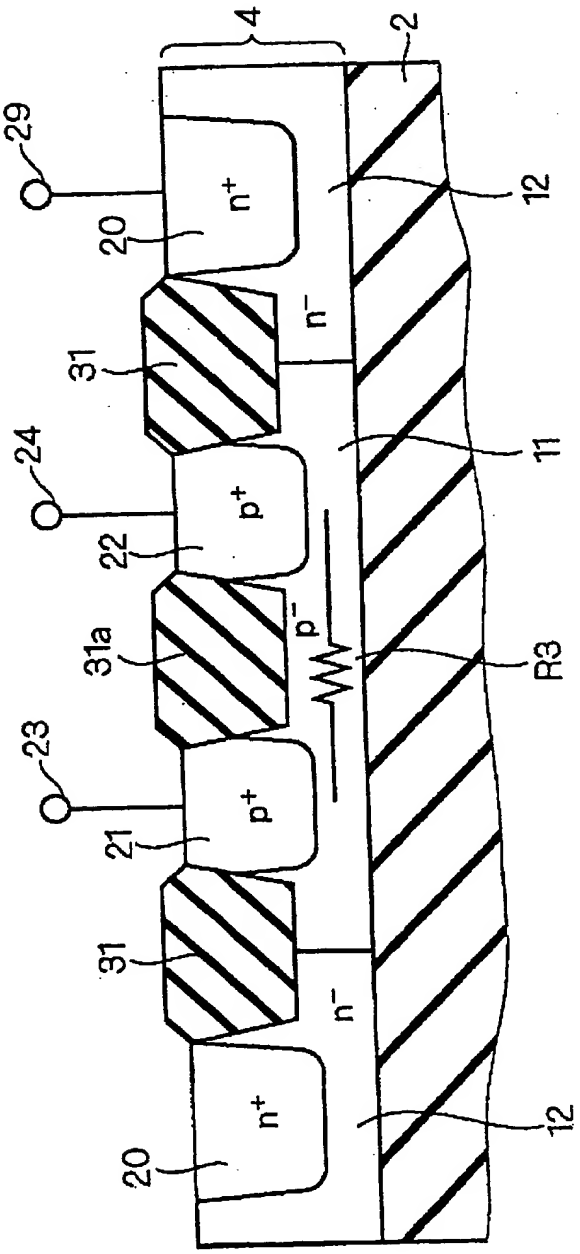
[FIG. 24]



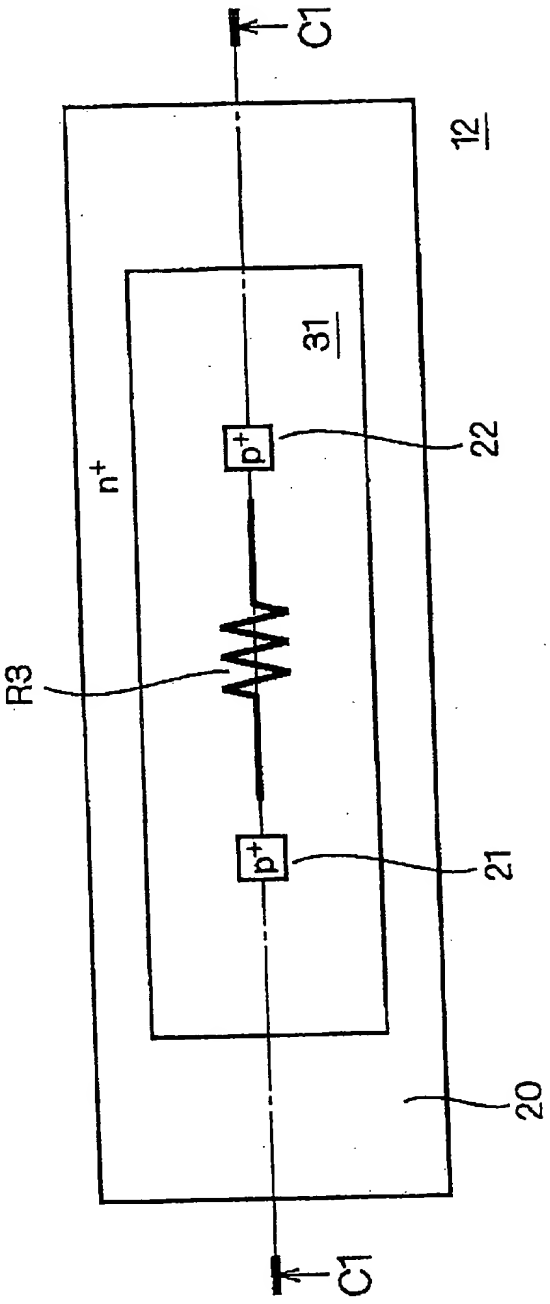
[FIG. 25]



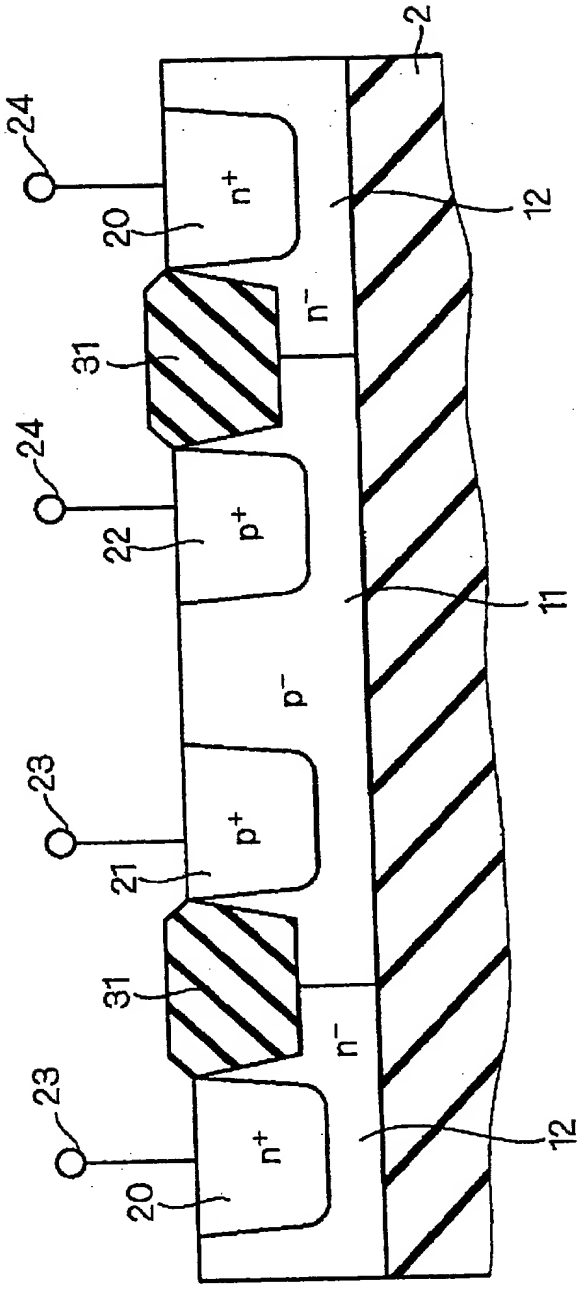
[FIG. 26]



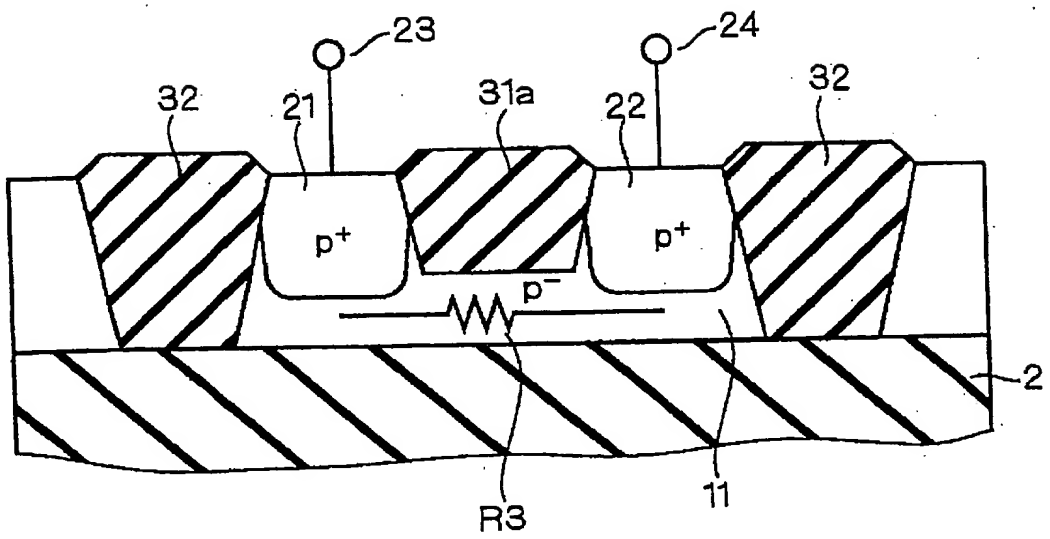
[FIG. 27]



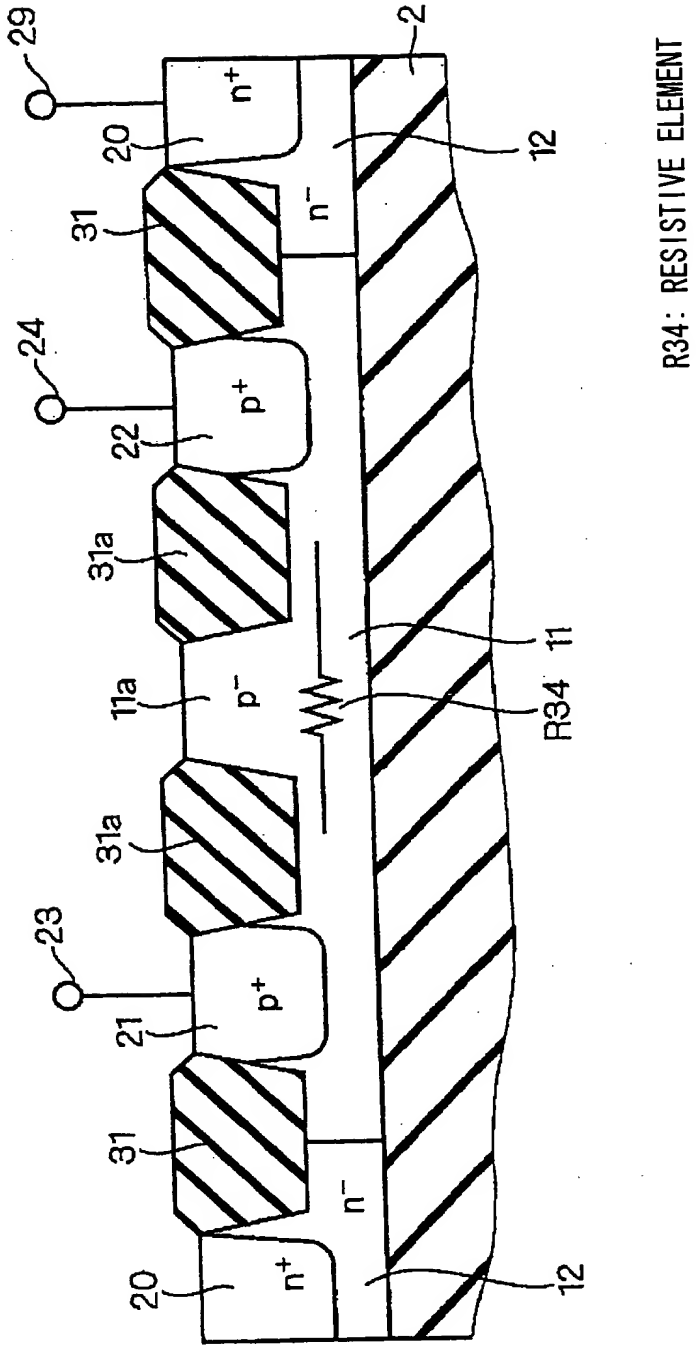
[FIG. 28]



[FIG. 29]

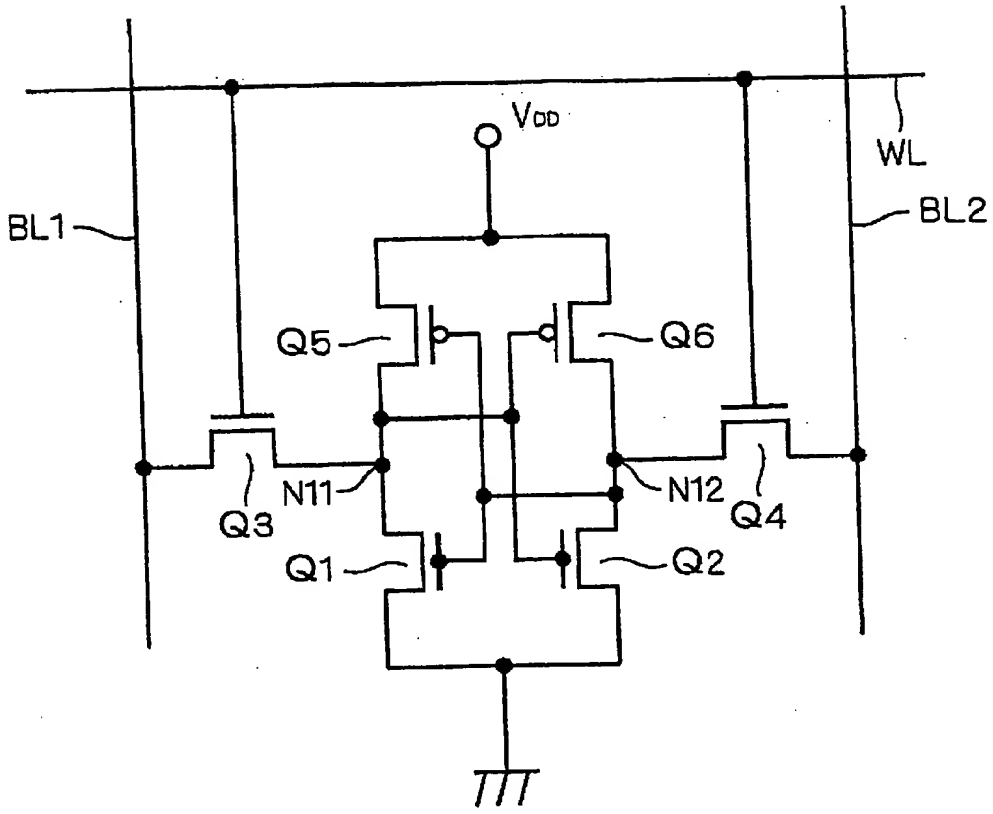


[FIG. 30]

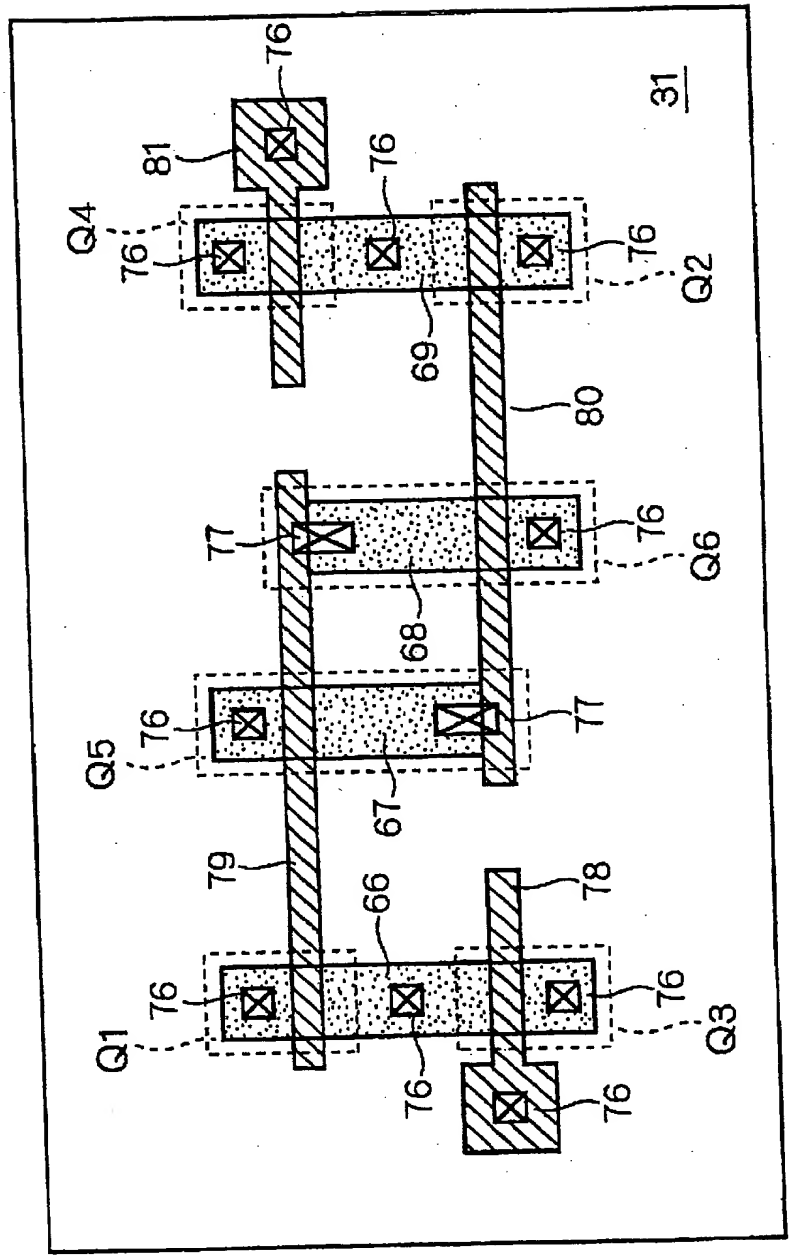


R34: RESISTIVE ELEMENT

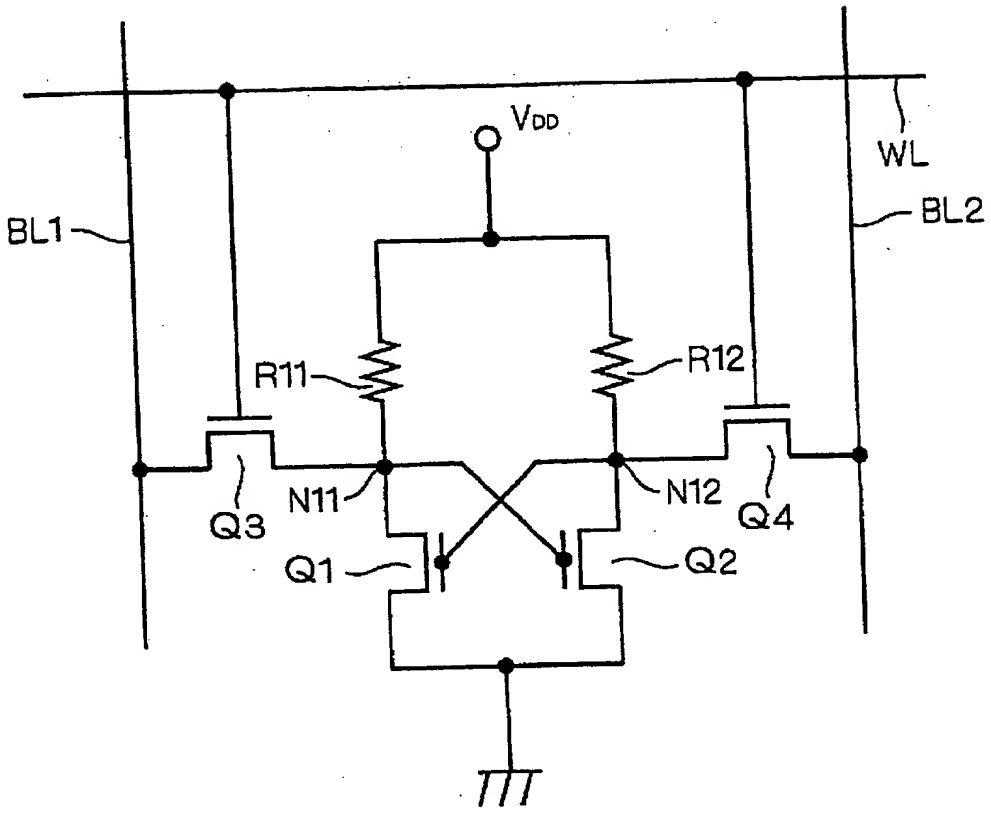
[FIG. 31]



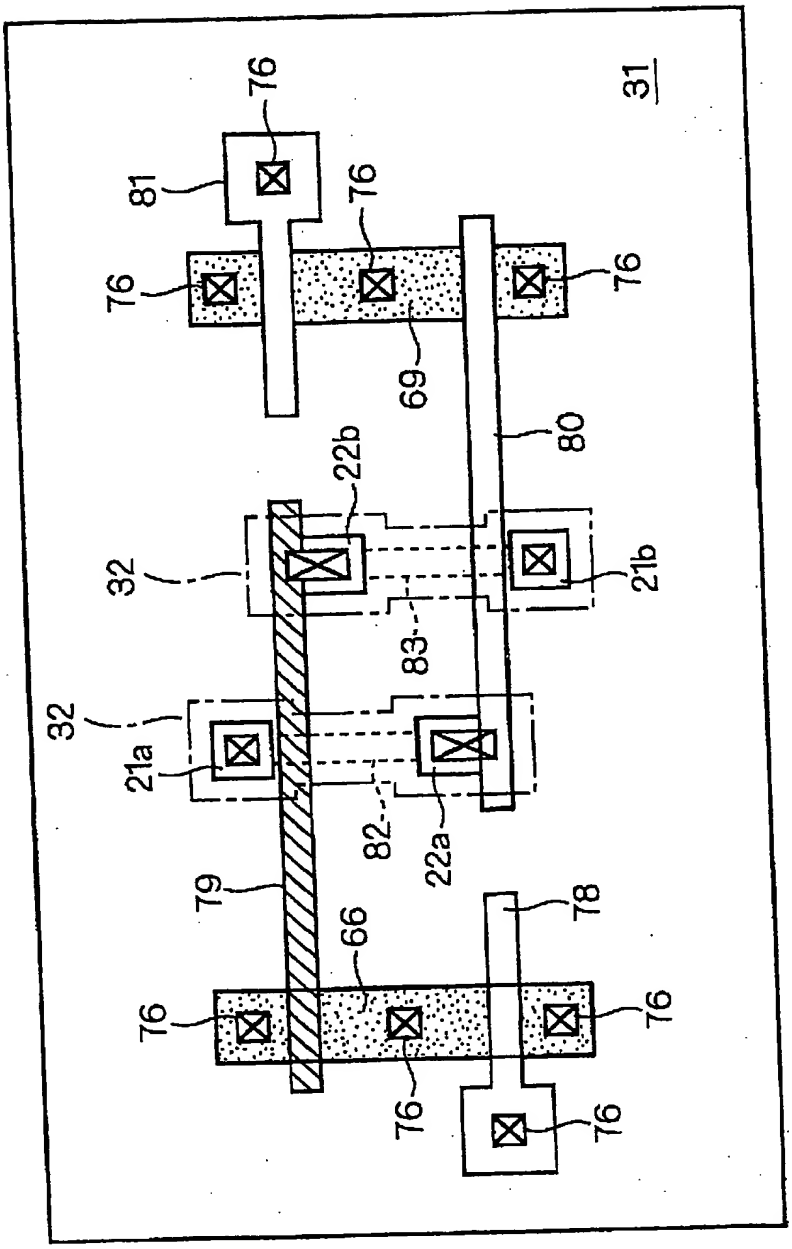
[FIG. 32]



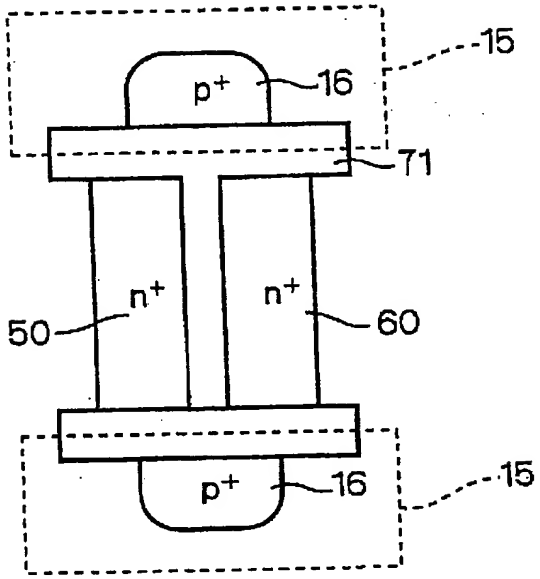
[FIG. 33]



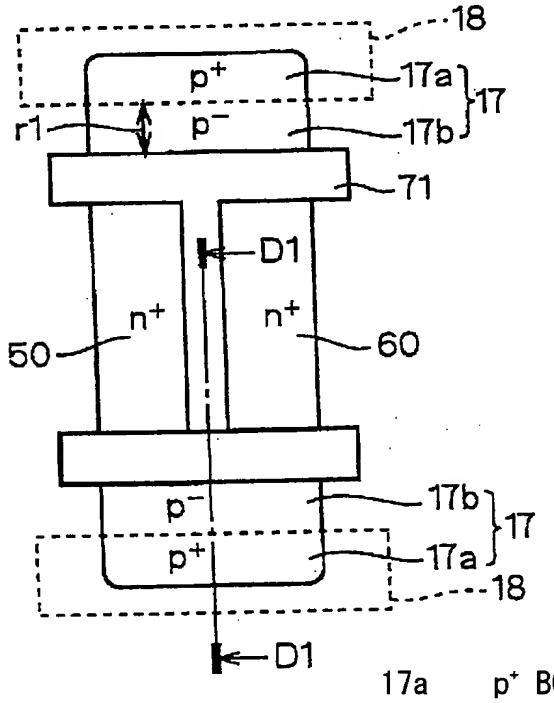
[FIG. 34]



[FIG. 35]

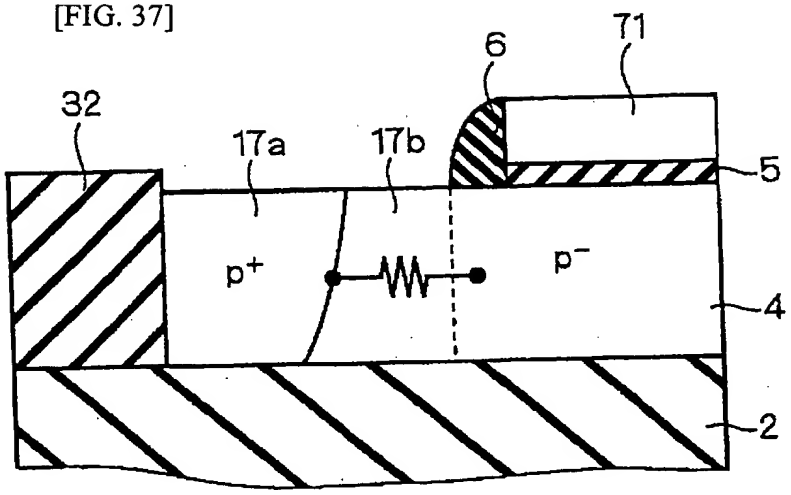


[FIG. 36]

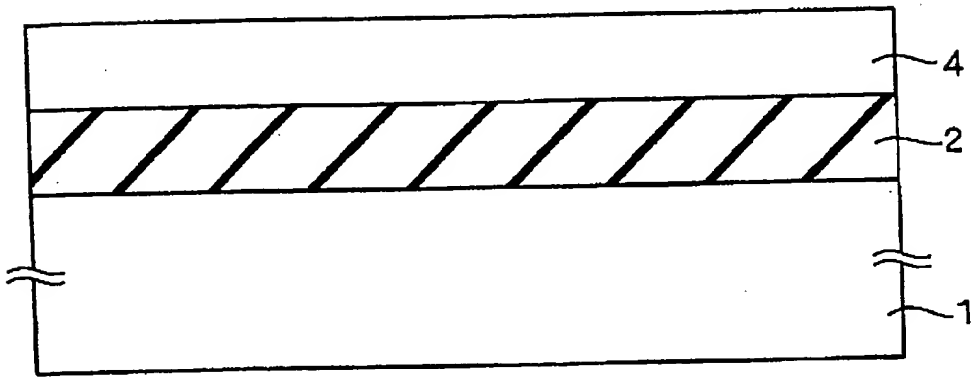


17a p+ BODY REGION
17b p- BODY REGION

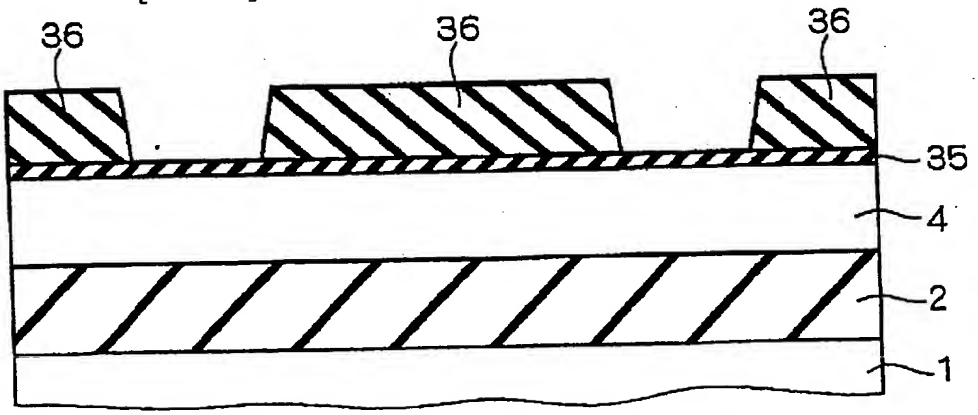
[FIG. 37]



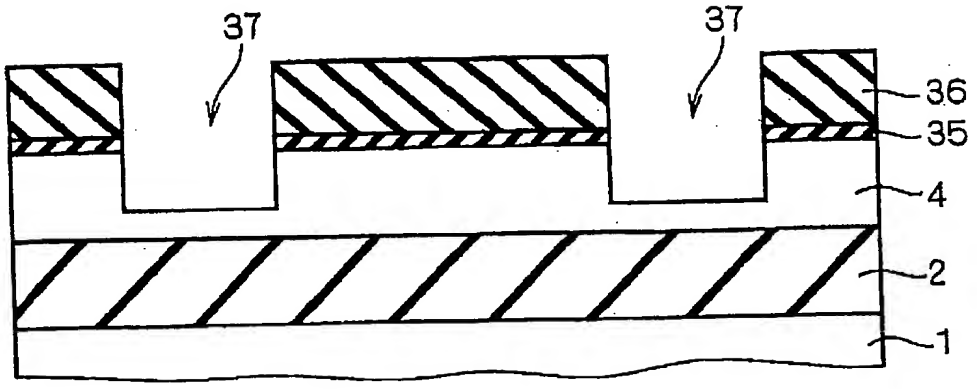
[FIG. 38]



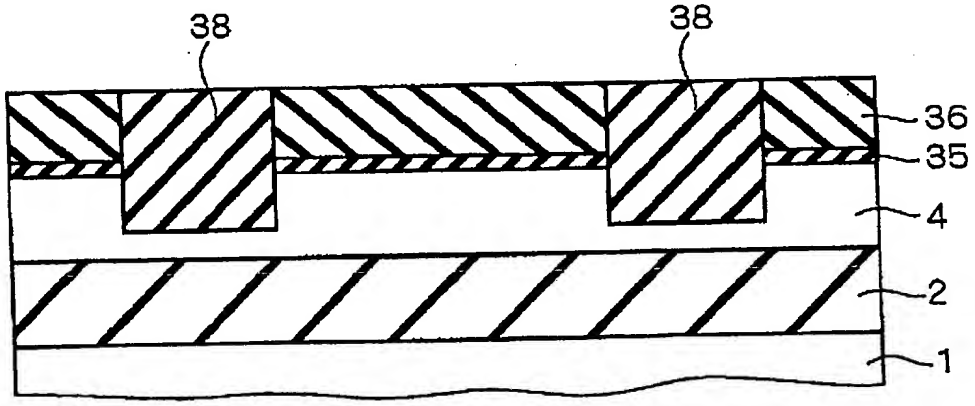
[FIG. 39]



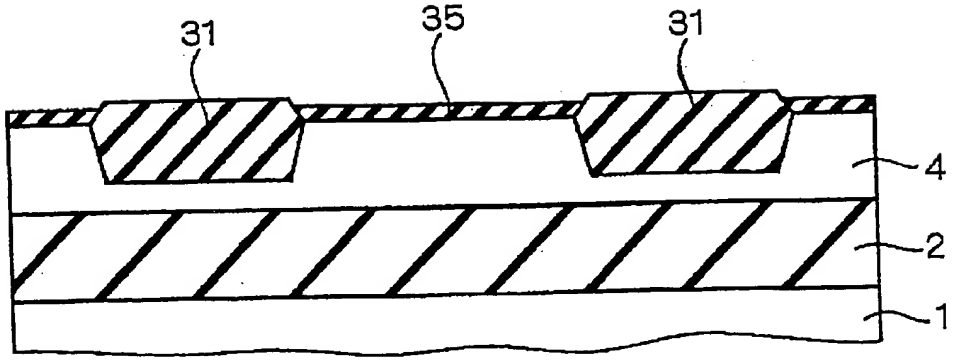
[FIG. 40]



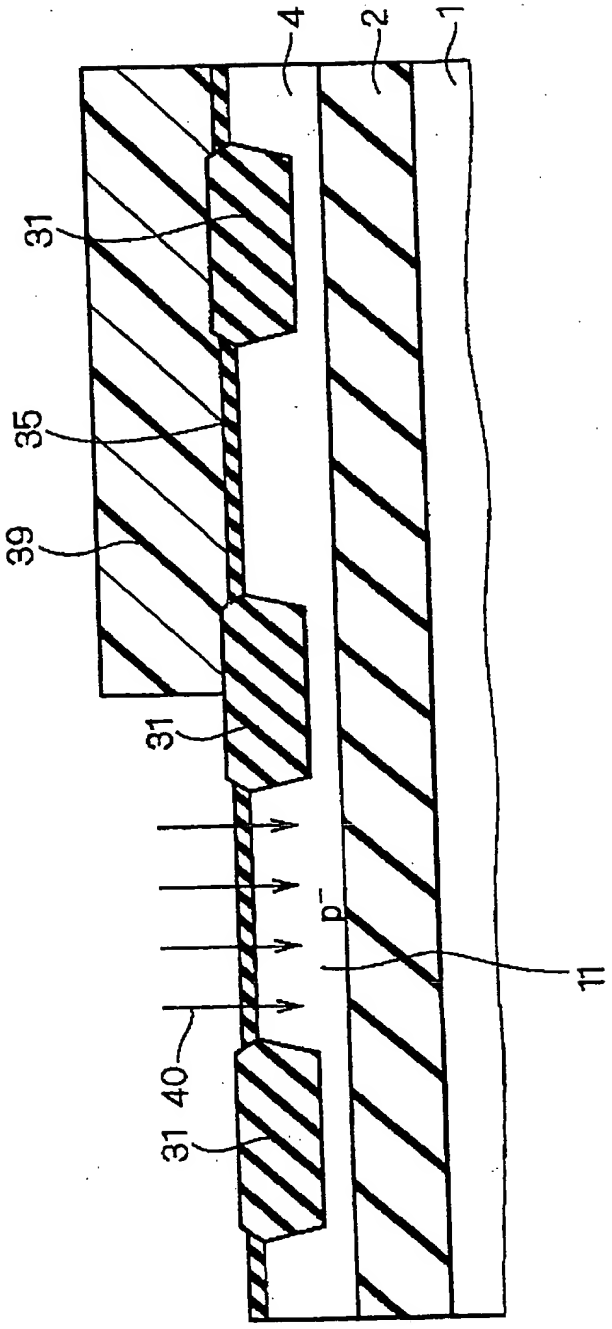
[FIG. 41]



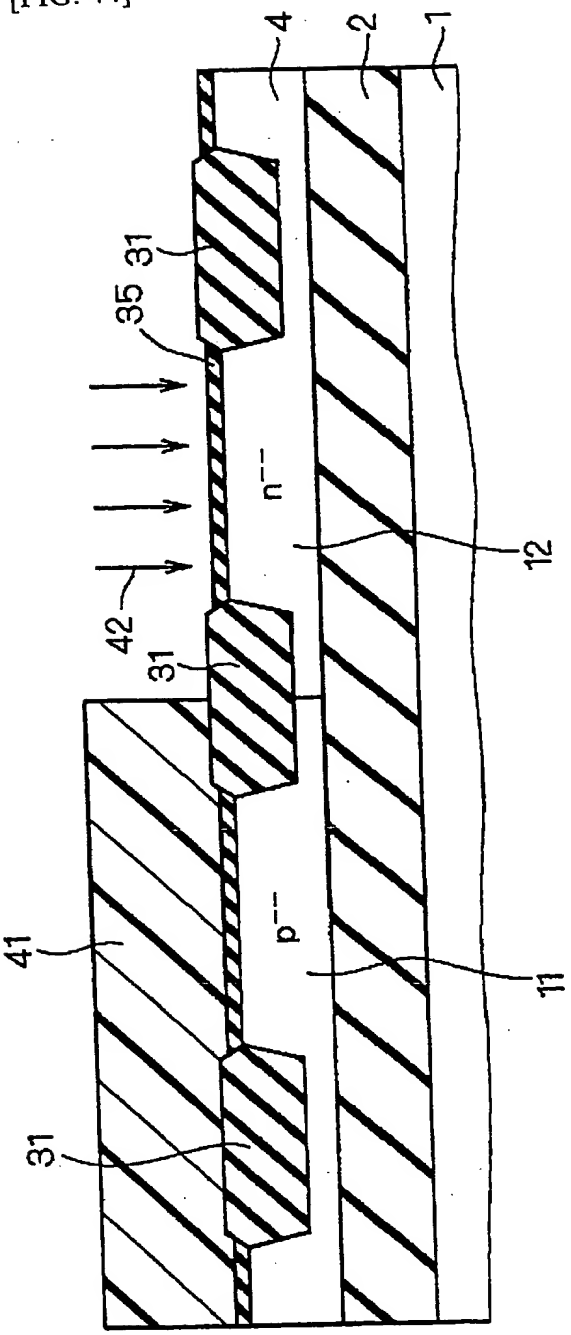
[FIG. 42]



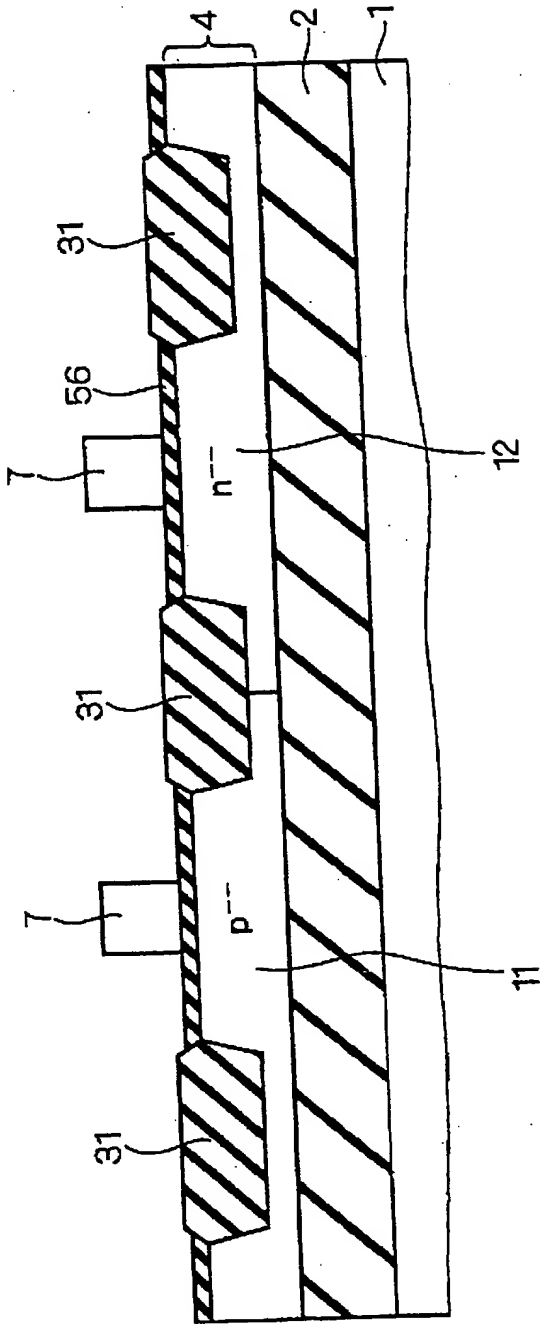
[FIG. 43]



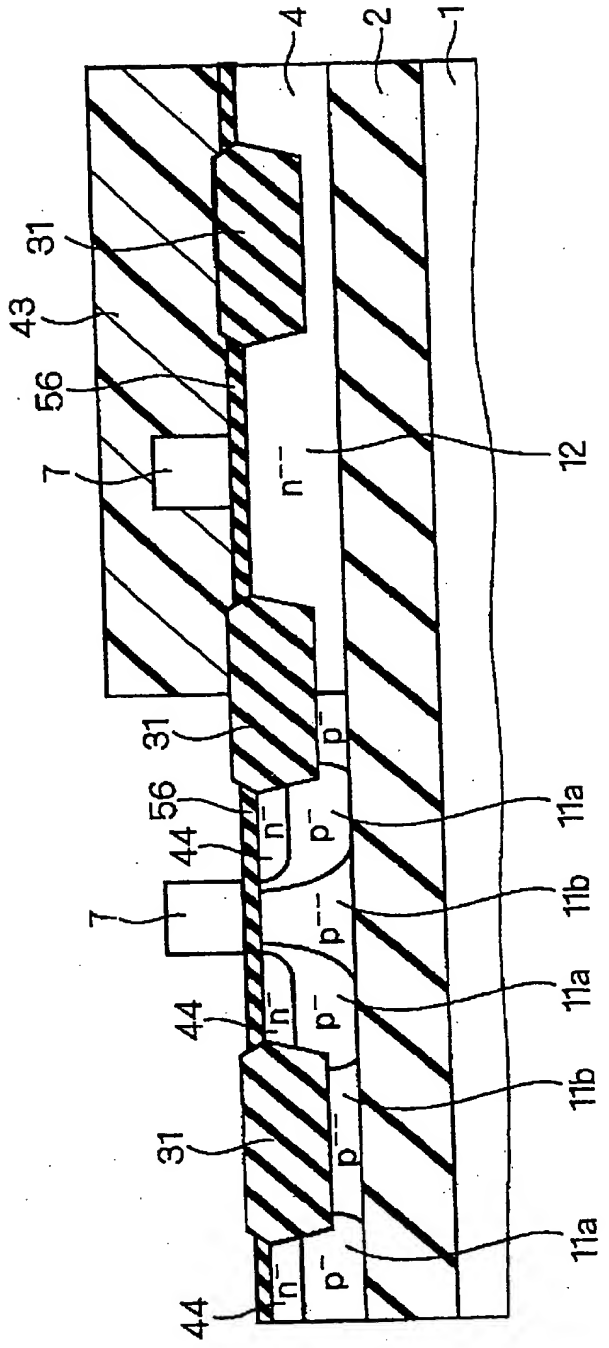
[FIG. 44]



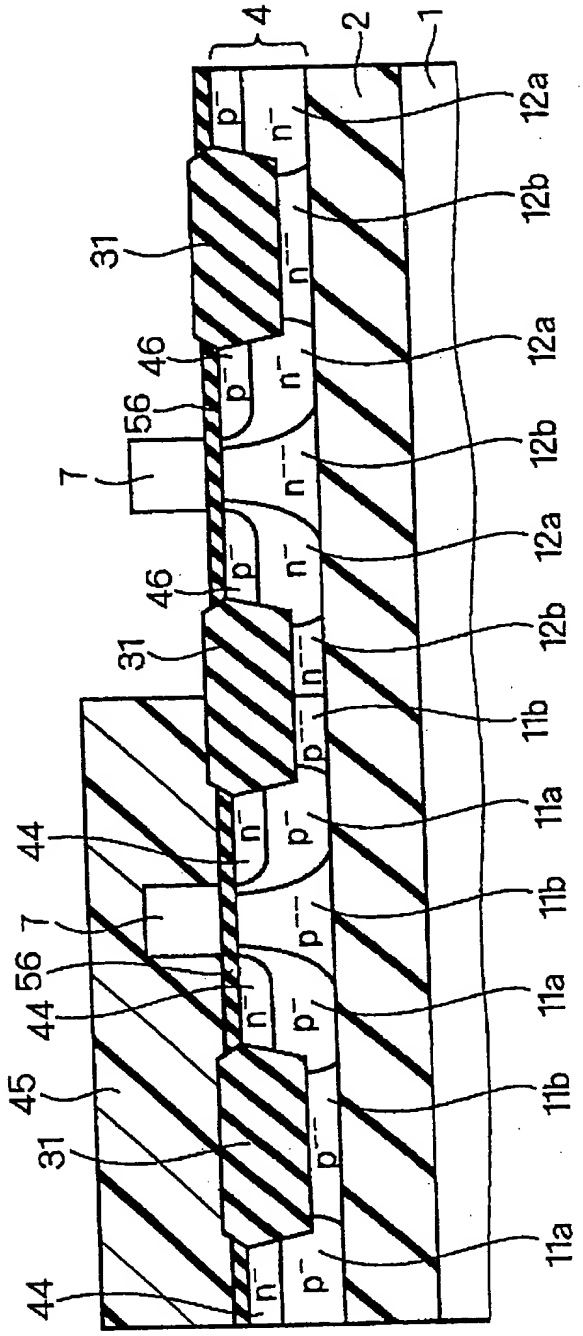
[FIG. 45]



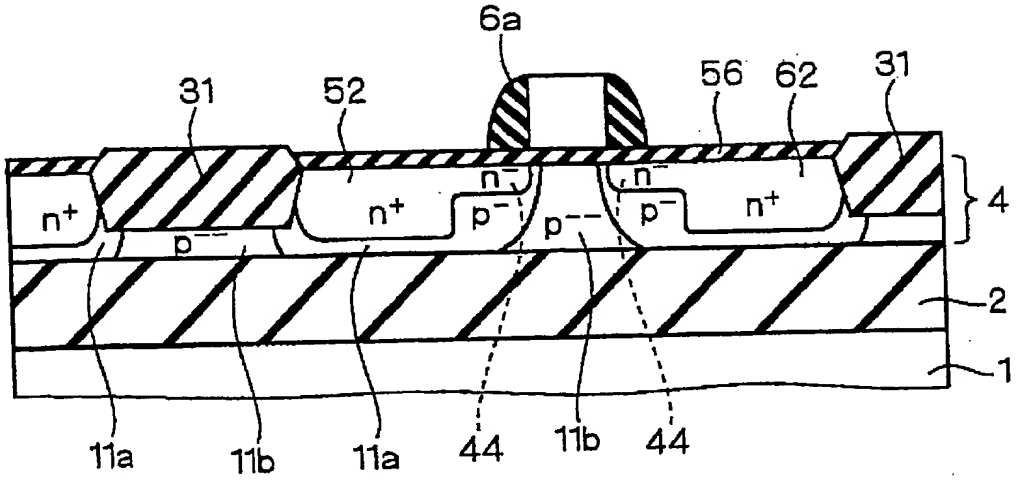
[FIG. 46]



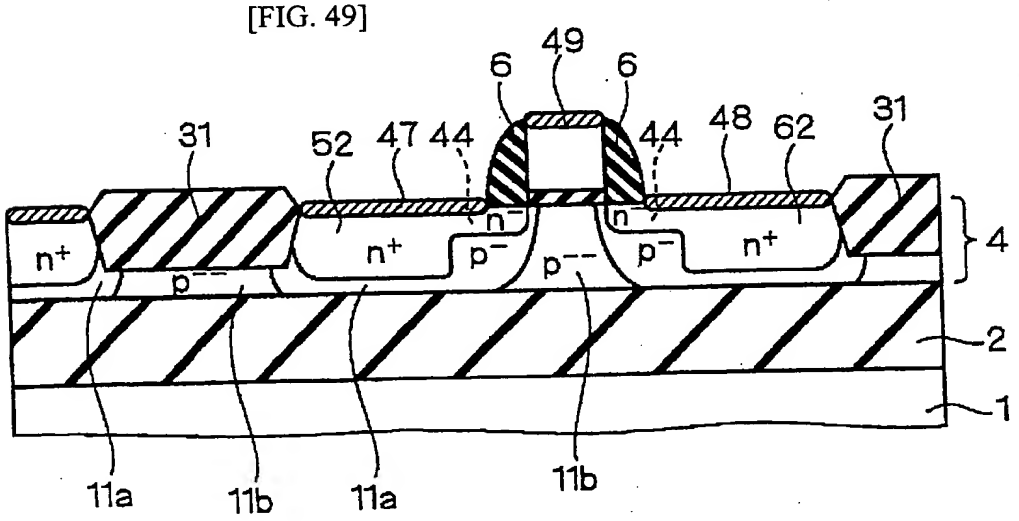
[FIG. 47]



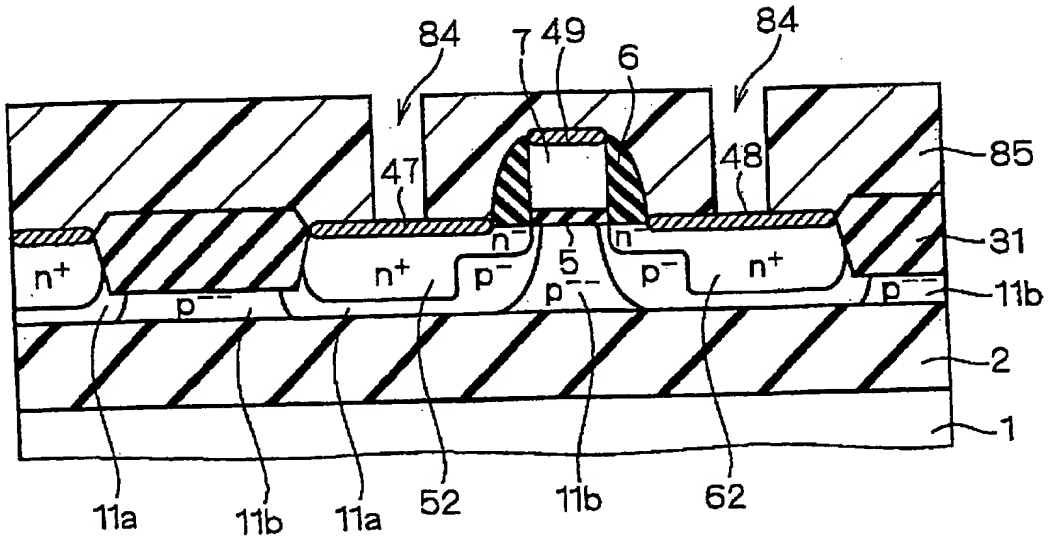
[FIG. 48]



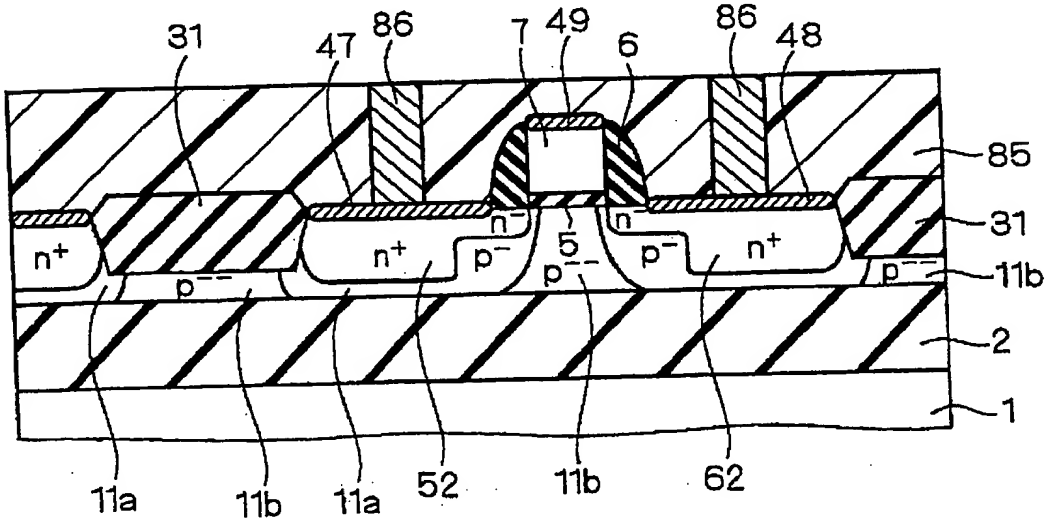
[FIG. 49]



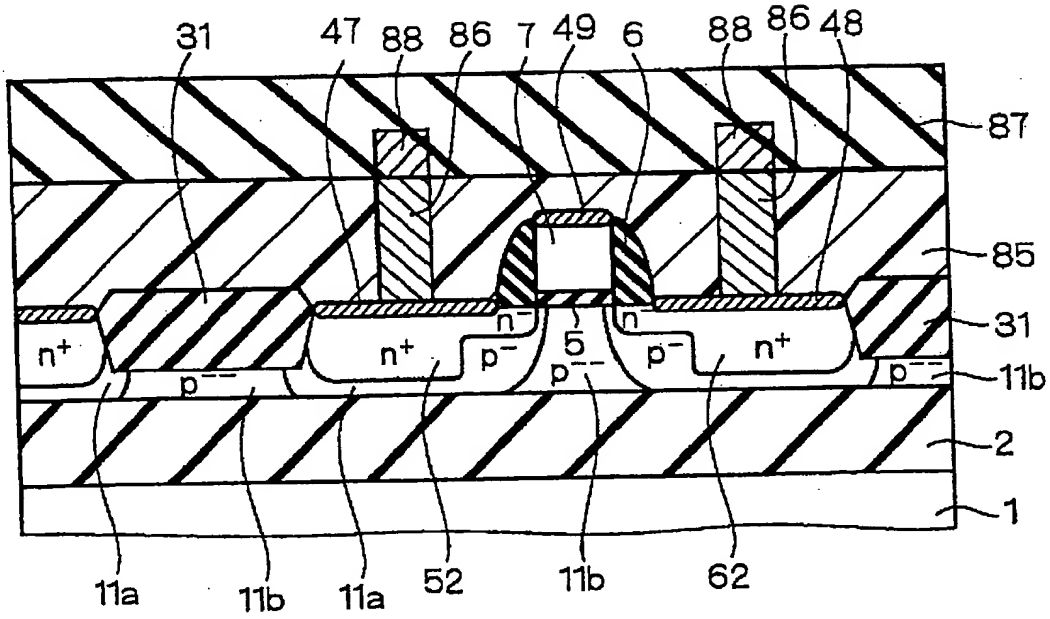
[FIG. 50]



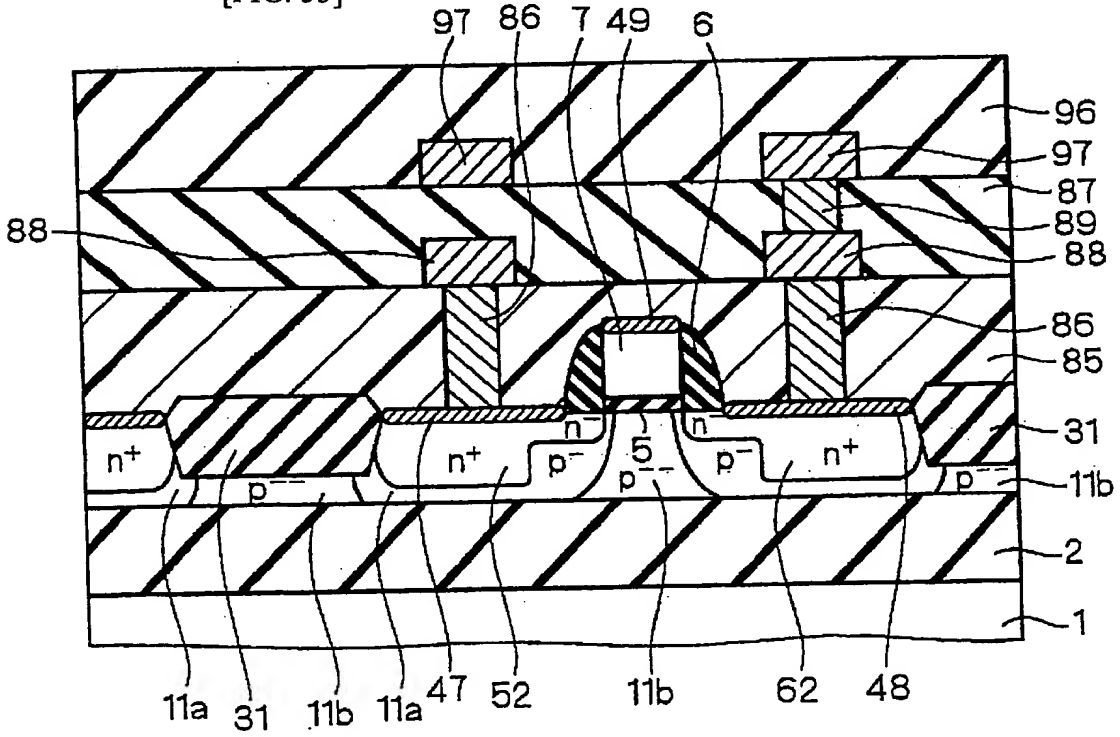
[FIG. 51]



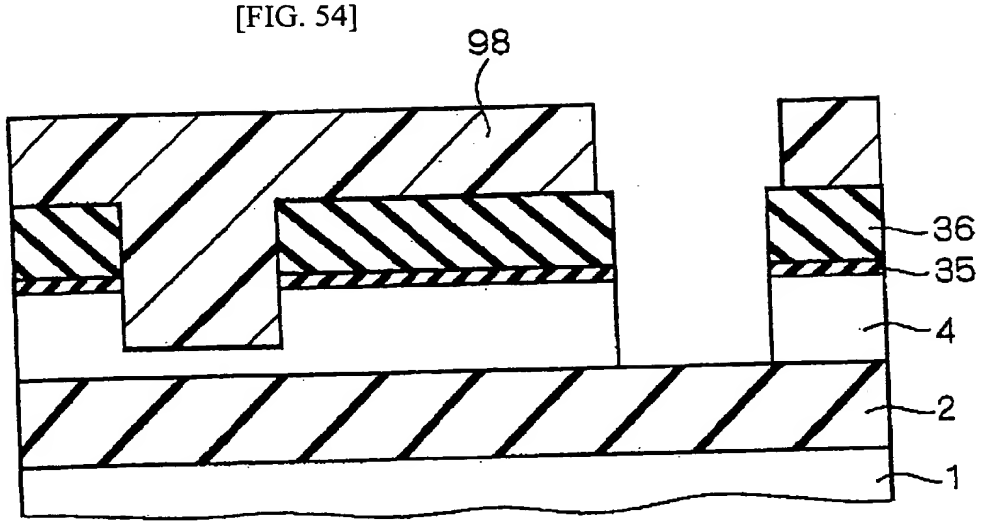
[FIG. 52]



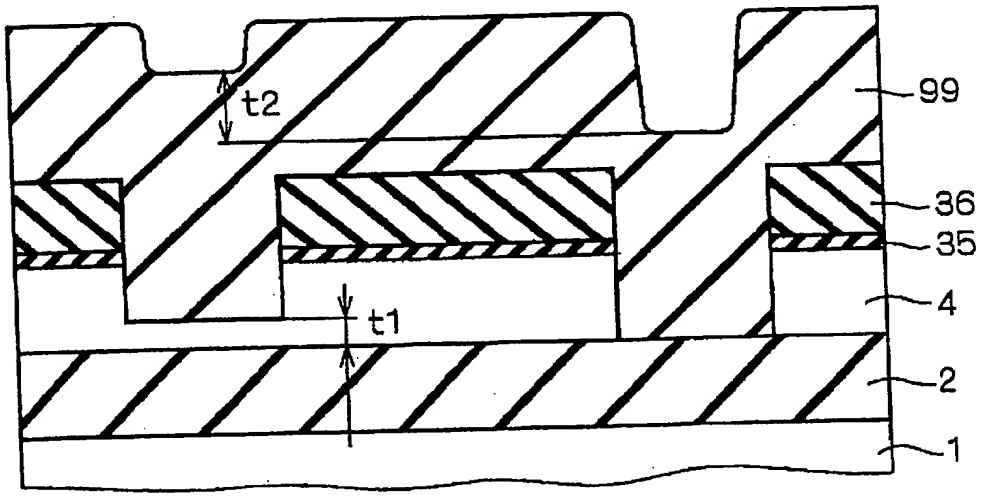
[FIG. 53]



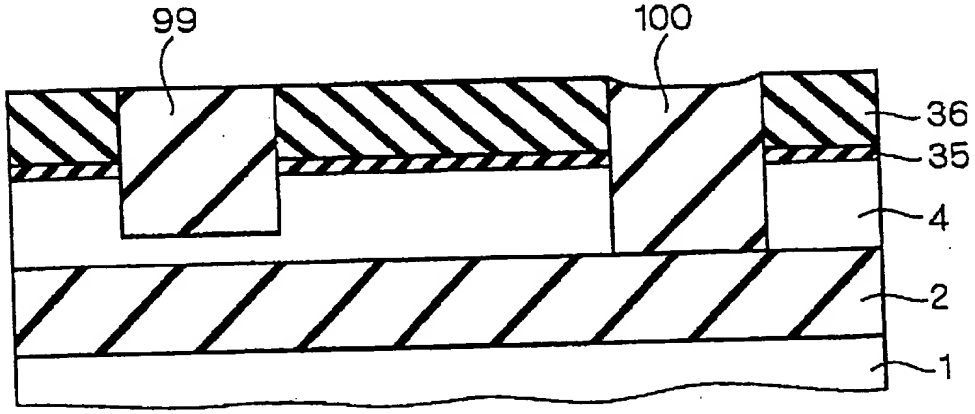
[FIG. 54]



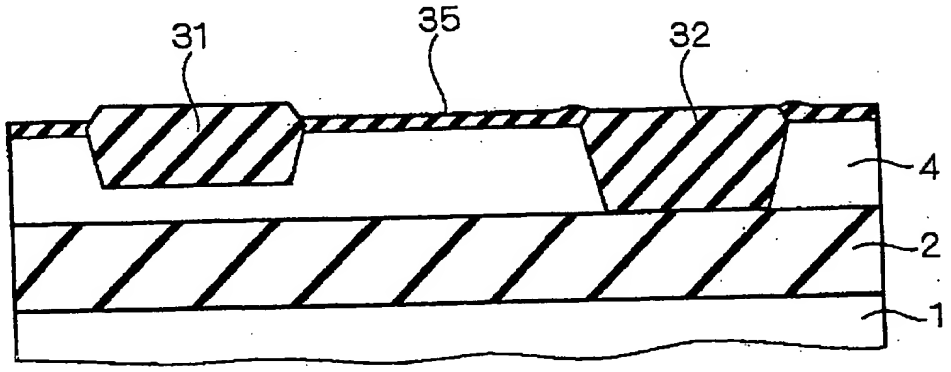
[FIG. 55]



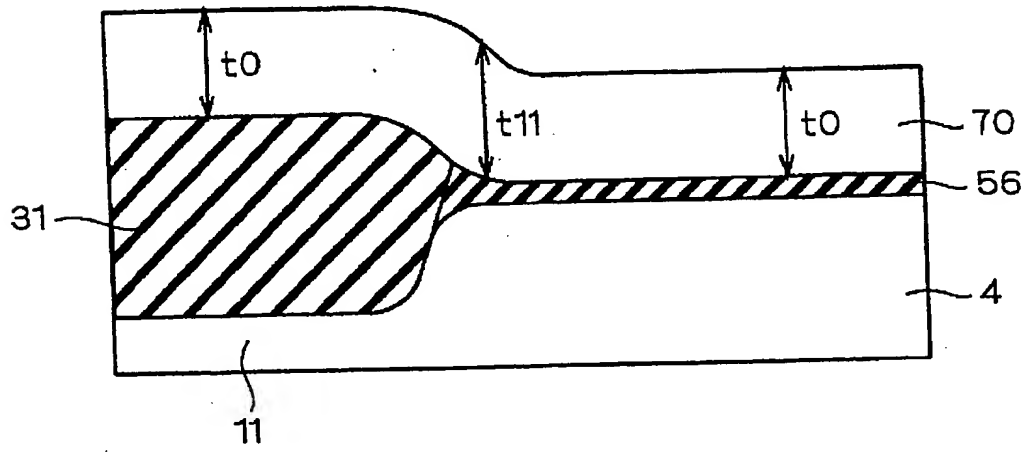
[FIG. 56]



[FIG. 57]



[FIG. 58]



[FIG. 59]